1. (5 points)
Given Boolean function \( F(A,B,C,D) = \Sigma m(1,5,9,11) \) with don’t-care condition \( d(A,B,C,D) = \Sigma m(3,8,10,13) \), where \( \Sigma m(1,5,9,11) \) is the standard sum of minterms format: \( m_1 + m_5 + m_9 + m_{11} = A'B'C'D + A'BC'D + AB'C'D + ABC'D \).
Implement \( F \) with the minimum number of AND, NOT, and OR gates. Draw the single-rail circuit implementation where only the primary inputs are available.

2. (5 points)
Implement a full adder using two 4 x 1 multiplexers. No logic gates are allowed. Both primary inputs and their complements are available to the multiplexers.

3. (6 points)
Design a sequential circuit that generates the following periodic repetition of binary sequence: 5, 3, 1, 7, 2, one digit at each clock cycle. Use T flip-flops and logic gates.
(1) Draw the state diagram of this system.
(2) Derive the flip-flop input function for each of the flip-flops in the sum of products format with the minimum number of literals.
(3) Draw the logic diagram of this sequential circuit.
(4) Discuss whether your design is self-correcting.

4. (4 points)
Analyze the following sequential circuit (\( o \) next to the flip-flop indicates an inverter).
(1) Draw the state table.
(2) Give a high level specification of the circuit.
1. $F(A, B, C, D) = B'D + C'D = (BC)'D$

2. Full adder,
   \[ S = x \oplus y \oplus c \]
   \[ C = xy + \bar{x}y + yc \]

3. (1) \[ 5 \rightarrow 3 \rightarrow 1 \rightarrow 5 \rightarrow 2 \]
   (2) \[ TA = A \oplus B' + c' \]
   \[ TB = A' \oplus B' \]
   \[ TC = c' + AB \]
   (3) the design is self-correcting

4. (1) \[
\begin{array}{ccc}
A_1 & A_2 & A_3 \\
0 & 0 & 0 \\
1 & 0 & 0 \\
0 & 1 & 0 \\
1 & 1 & 0 \\
0 & 0 & 1 \\
1 & 0 & 1 \\
0 & 1 & 1 \\
1 & 1 & 1 \\
0 & 0 & 0
\end{array}
\]
   (2) a mod-8 up counter if we read output in the order of $A_3, A_2, A_1$
   or this is a frequency divider

(next state is shown in the next line)