Digital Logic – ECE Written Qualifying Examination – Fall 2015

1. (5 points)
   Consider Boolean expression \((w' + x)y + (u' + v)(w + z)y\)
   (a) Draw the logic diagram of the \{AND, OR\} circuit that directly implements this expression. That is, do not change or simplify the expression and use only AND and OR gates. You can assume that both a variable and its complement can be used directly.

   (b) Convert the \{AND, OR\} circuit from part (a) to a circuit with only NAND gates, again assuming that both a variable and its complement can be used directly. It is sufficient to draw the logic diagram. No need to show how to do the conversion.
2. (3 points, 0.5 point each) Write your answer on the provided space.
Consider the function \( f(w,x,y,z) \) implemented by the MUX tree, determine the value or the expression of the followings: ( \( \overline{x} \) is the complement of \( x \), the same as \( x' \) )

\[
\begin{align*}
f(1,0,0,1) &= \underline{\text{__________}} \\
f(0,1,1,0) &= \underline{\text{__________}} \\
f(w,1,1,1) &= \underline{\text{__________}} \\
f(w,0,1,1) &= \underline{\text{__________}} \\
f(1,0,y,0) &= \underline{\text{__________}} \\
f(0,x,1,z) &= \underline{\text{__________}}
\end{align*}
\]

3. (2 points)
Prove that \((x+y) \odot (x+z) = x + (y \odot z)\), where \( x \odot y = (x \oplus y)' \) is the exclusive NOR operator. No point will be given if you use the truth table method.
4. (4 points)
Implement a D flip-flop with one T flip-flop and other necessary logic gates. Draw the logic diagram to show your implementation.
(Note: T flip-flop’s next state is given by $Q(t+1) = T \oplus Q(t)$; D flip-flop’s next state is given by $Q(t+1) = D$)
5. (6 points)
The following sequential circuit has one T flip-flop and one D flip-flop, one input x that can be 0 or 1, two logic AND gates, and a clock pulse CP.

(a) Starting with T=0 and D=1, find an input value or a sequence of input values for x to transit the circuit state to T=0 and D=0. If you believe that there is no such input or input sequence that can make this transition happen, explain why. We refer to \{T=0, D=1\} as the initial state 01, and \{T=0, D=0\} as the ending state 00.

(b) Repeat part (a) with initial state 11 and ending state 01.

(c) Repeat part (a) with initial state 10 and ending state 00.
Q2

1, 0, w, o, y, x + x'

Q3

\[(x + y) \odot (x + z) = (x + y)(x + z) + (x + y)'(x + z)'
\]

\[= x + y z + x' z'
\]

\[x + (y \odot z) = x + (y z + y' z')
\]

\[= x + y z + y' z'
\]

\[= x + y z + x' y' z'
\]

so

\[(x + y) \odot (x + z) = x + (y \odot z)
\]
functionality of the D flip-flop to be designed

<table>
<thead>
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<th>D</th>
<th>cs.</th>
<th>ns.</th>
<th>T</th>
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<tbody>
<tr>
<td>0</td>
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input to the T flip-flop to enable the above transition, express T as a function of D input and current state

\[ T = D \oplus cs. \]

Q5

state transition graph of the circuit.

1. from state 01 to 00, set input \( x = 0 \)
2. from state 11 to 01, give input sequence 11 (or 101)
3. you cannot go from 10 to 00, because on any input value, state 10 stays at itself