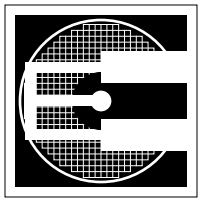


Midterm Exam (20%)

ENEE 359a: Digital VLSI Design, Spring 2007
The Ides of March, Opening Round of the NCAA Tournament

This exam should take you less than an hour: 5 questions, 10 minutes apiece. The exam is closed book, closed notes.

Note that each question is worth the same number of points; this means you should do those questions you find easy first.

Solutions

Name: _____

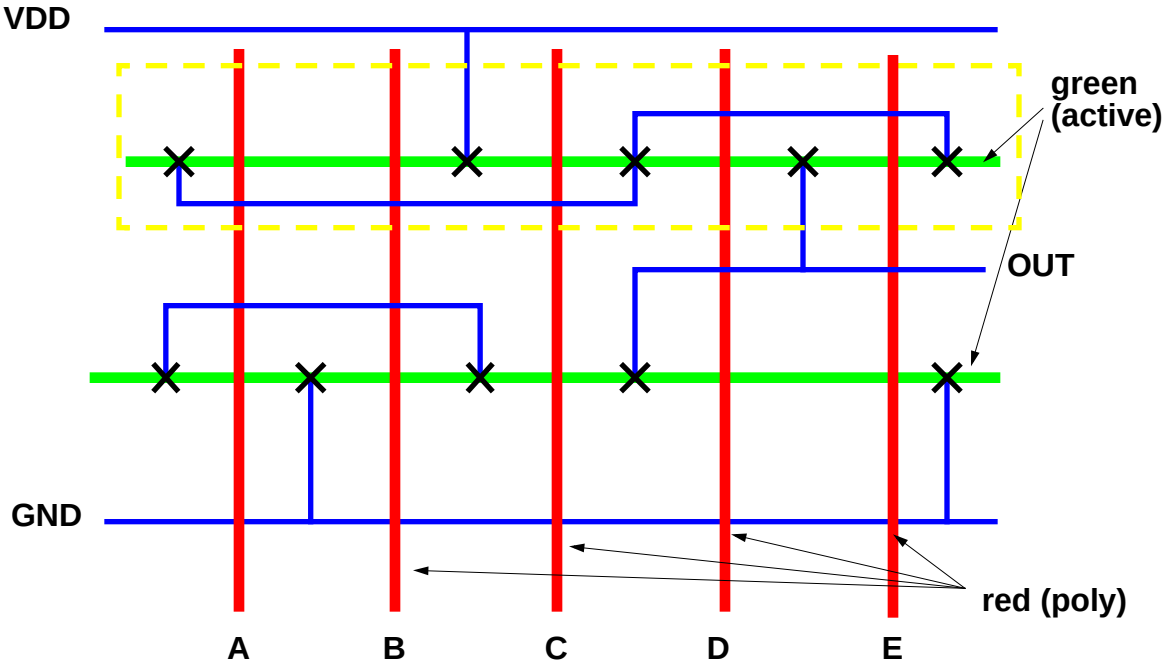
Score:

Problem 1:	out of 4
Problem 2:	out of 4
Problem 3:	out of 4
Problem 4:	out of 4
Problem 5:	out of 4
Total:	

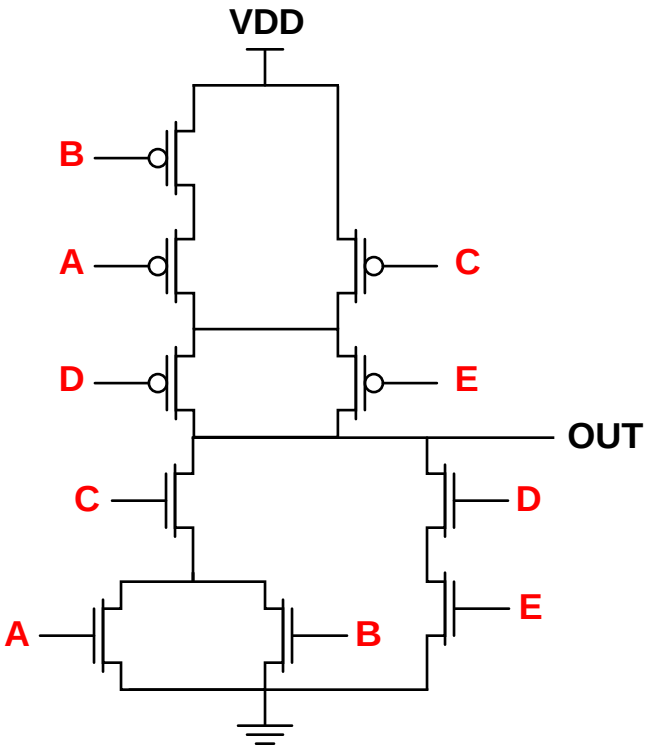
Grade Distribution:

20 - X X
19 - X X X X
18 - X X X
17 -
16 - X
15 - X X X
14 -
13 - X
12 -
11 -
10 -
9 - X

1. **Consider the following stick diagram. Draw the electrically equivalent transistor-level schematic. What logic equation does the circuit implement?**



solution:

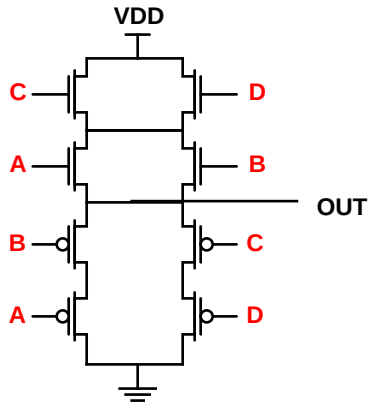


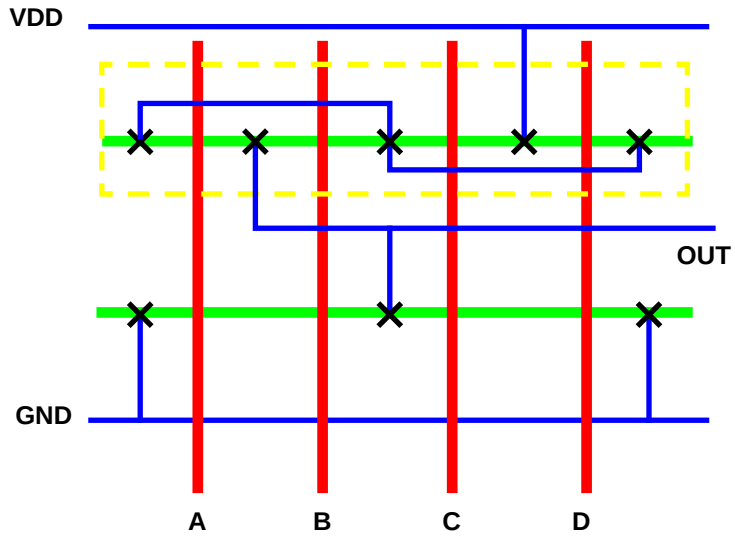
out = ~(DE + C(A+B))

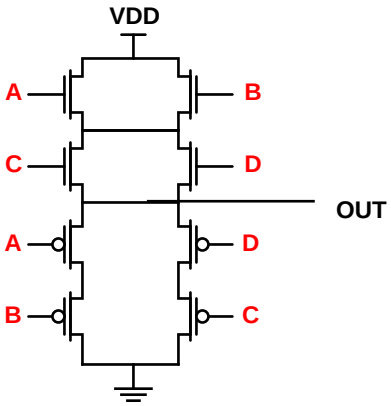
out = ~(DE + CA + CB)

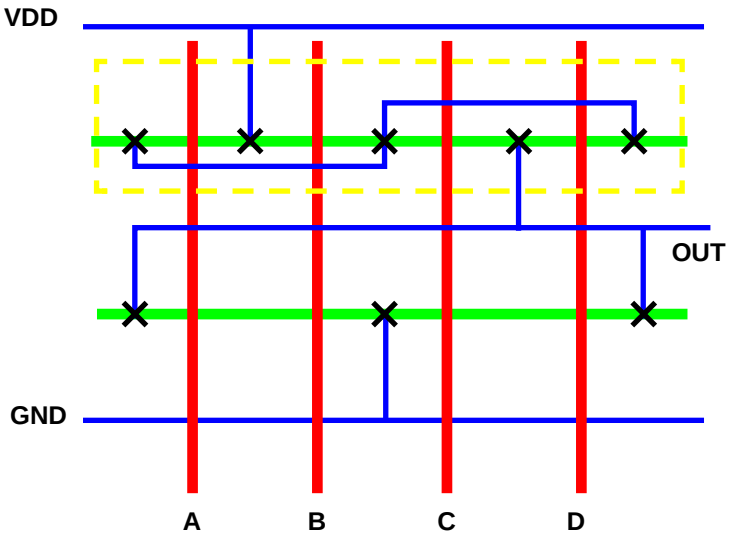
2. Consider the logical expression out = ~(ab + cd)**. Convert this to a schematic diagram for static CMOS logic, then convert it to a stick-diagram layout (as in question 1).**

some equivalent solutions (there is more than one correct answer):

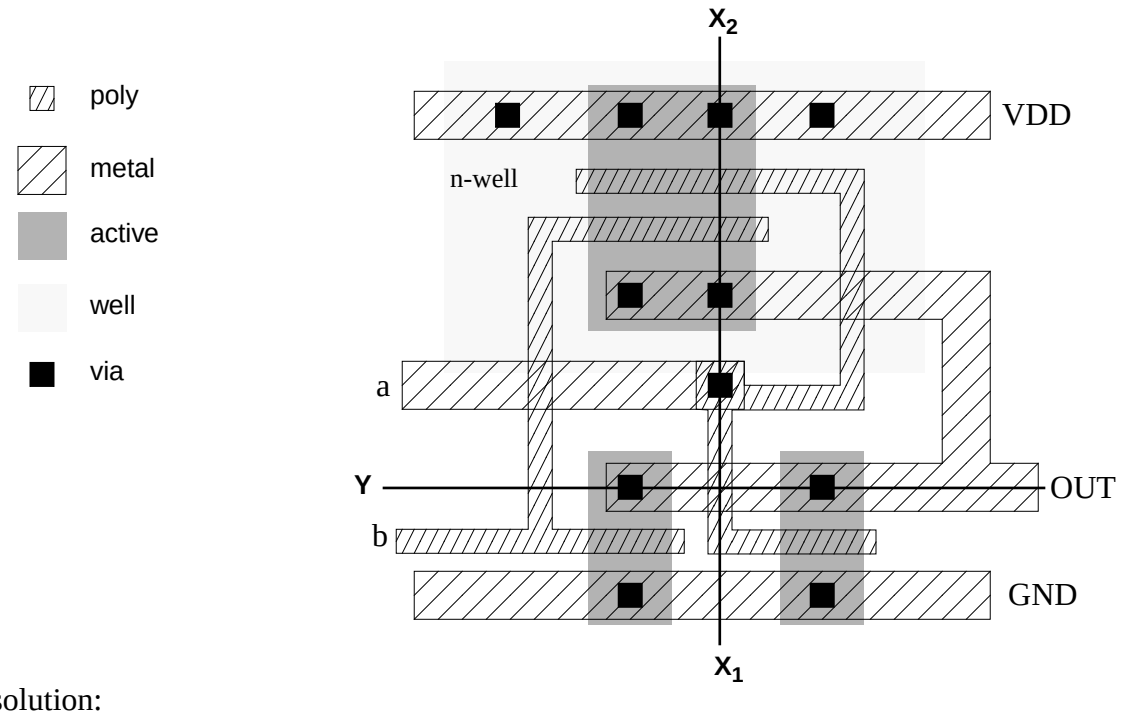




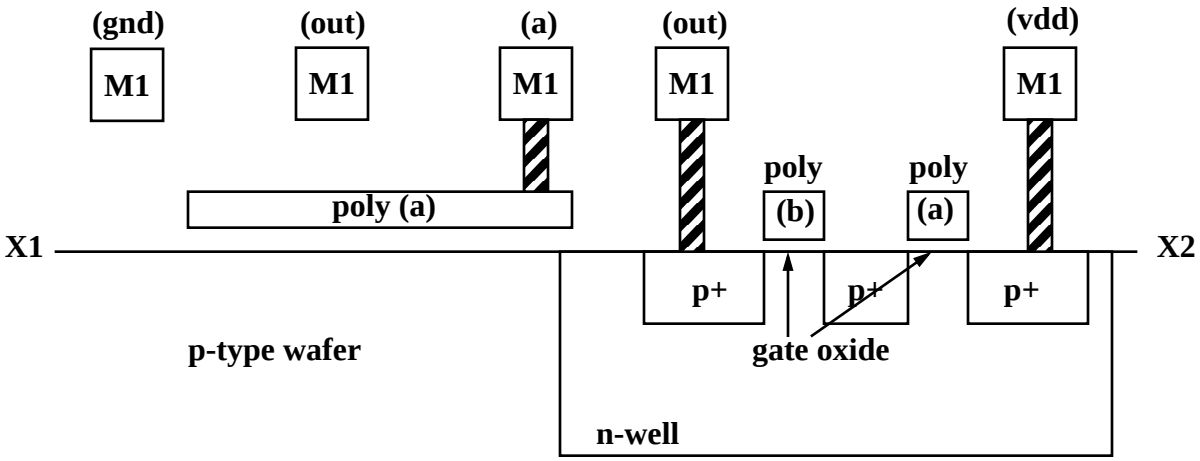


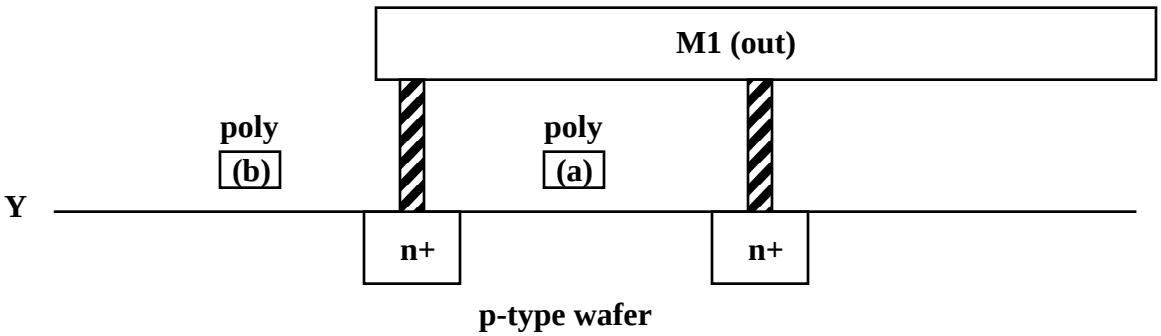


3. Provide a side-view diagram for each of the cuts X and Y through the layout below. Be sure to label each of the strata. Label your endpoints for the X cut, so it is clear which end is which.



solution:



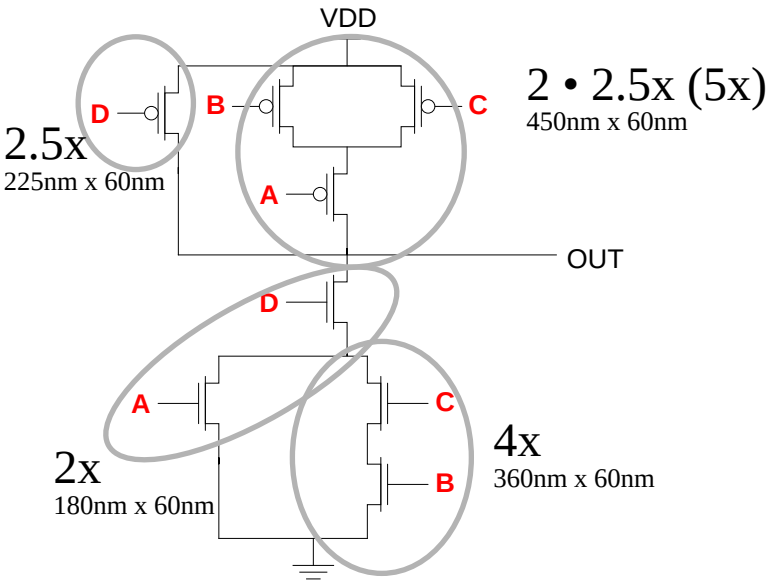


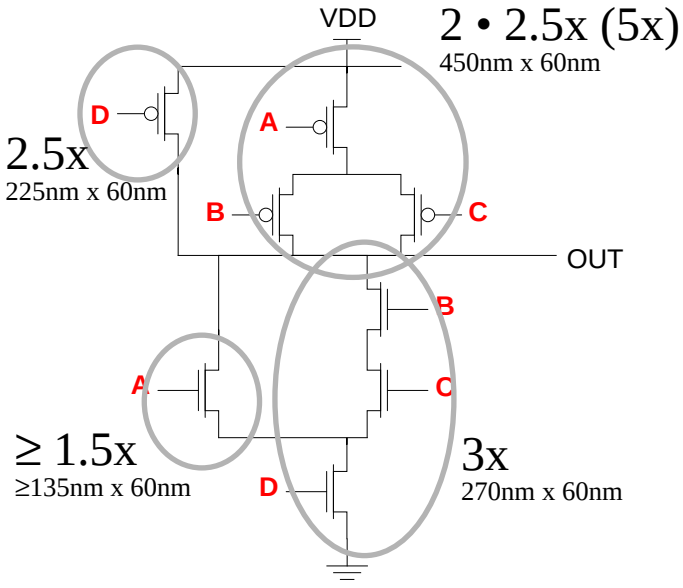
4. **Consider the function** out = ~((a + bc) • d)**. Draw the circuit and size the transistors: size all NMOS and PMOS transistors so that the PUN and PDN each has equivalent resistance to a minimum-sized MOSFET, and then take into account the fact that $\mu_n = r \cdot \mu_p$ where $r = 2.5$ (i.e. the resistance of a unit PMOS device is 2.5 times that of a unit NMOS device).**

Important: Assume the circuit is implemented in a 60nm technology and that the dimensions of a **minimum-sized MOSFET** in this technology are **90nm width x 60nm length**. Express the dimensions of each MOSFET in the optimized circuit in nanometers (W nm x L nm).
I.e., what is it that you are scaling?

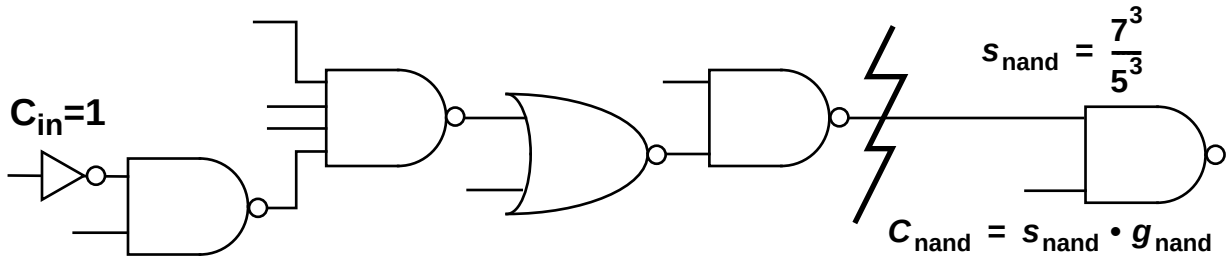
some equivalent solutions (there is more than one correct answer):

min. device: WxL = 90nm x 60nm





5. You have identified a critical path through a circuit, as shown below. Consider the path up to the jagged line; the 2-input NAND beyond simply represents the load being driven (it can be thought of as the input to a D-latch, for example). That NAND has been scaled by a factor of $7^3 \div 5^3$ which can be approximated by the value 2.8. Thus, the load NAND has C_{nand} approximately equal to 3.5 C_{in}. Find the scaling terms s_i for each gate and the optimized path delay. Assume that gamma=1, that r=3, and that the p_i terms are all equal (leave as "p").



Equations you might find useful:

Optimal gate effort h $= \sqrt[N]{GFB} = \sqrt[N]{H}$

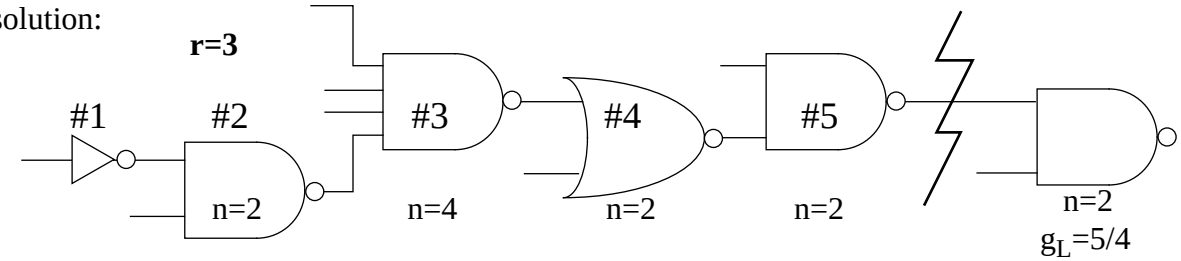
Delay through path $= t_{p0}\sum\left(p_i + \frac{f_i g_i}{\gamma}\right)$

$g_{nand} = \frac{n+r}{1+r}$ $g_{nor} = \frac{1+nr}{1+r}$ $f_{i,opt} = \frac{h}{g_i}$

Optimal delay $= t_{p0}\left(\sum p_i + \frac{N\sqrt[N]{H}}{\gamma}\right)$

Sizing for gate i $= \left(\frac{g_1 s_1}{g_i}\right)\prod_{j=1}^{i-1}\left(\frac{f_j}{b_j}\right)$ $F = \frac{C_{load}}{C_{in}}$ $G = \prod_i g_i$

solution:



g_1=1 g_2=5/4 g_3=7/4 g_4=7/4 g_5=5/4 $C_L=7^3/5^3 \bullet 5/4$

$$h = \sqrt[N]{GFB} = \sqrt[5]{\left(1 \cdot \frac{5}{4} \cdot \frac{7}{4} \cdot \frac{7}{4} \cdot \frac{5}{4}\right) \cdot \left(\frac{7^3 \cdot 5}{5^3 \cdot 4}\right)} = \sqrt[5]{\left(\frac{7^5 \cdot 5^3}{5^3 \cdot 4^5}\right)} = \frac{7}{4}$$

$f_1 = \frac{7/4}{1}$ $f_2 = \frac{7/4}{5/4}$ $f_3 = \frac{7/4}{7/4}$ $f_4 = \frac{7/4}{7/4}$ $f_5 = \frac{7/4}{5/4}$ $\left(f_i = \frac{h}{g_i}\right)$

=7/4 =7/5 =1 =1 =7/5

$s_1 = 1$ $s_2 = \frac{1}{5/4} \cdot \frac{7}{4}$ $s_3 = \frac{1}{7/4} \cdot \frac{7}{4} \cdot \frac{7}{5}$ $s_4 = \frac{1}{7/4} \cdot \frac{7}{4} \cdot \frac{7}{5} \cdot 1$ $s_5 = \frac{1}{5/4} \cdot \frac{7}{4} \cdot \frac{7}{5} \cdot 1 \cdot 1$

= 7/5 **= 7/5** **= 7/5** **= 49/25 ≈ 2**

Delay $= t_{p0}\left(\sum p_i + \frac{N\sqrt[N]{H}}{\gamma}\right) = \boldsymbol{t_{p0}\left(5p + \frac{35}{4}\right)}$