



# Course Syllabus

ENEE 359a: Digital VLSI Circuits, Spring 2007

Prof. Bruce Jacob

## 1. Basic Information

### Time & Place

Lecture: TuTh 2:00–3:15 pm, EGR-3114

Discussion Section: Wed 12:00–12:50pm, EGR-1102

### Professor

Bruce L. Jacob: AVW-1325, blj@ece.umd.edu

Office hours: *Open-Door Policy (for now ...)*

### Teaching Assistant

Elliott Cooper-Balis, ecc17@umd.edu

### Class Home Page

<http://www.ece.umd.edu/courses/enee359a/>

### Class Email List

enee359a-0101-spring07@coursemail.umd.edu

### Class Schedule

This is a weekly schedule of my hours, including class time and scheduled office hours, but also including other things that make me unavailable. It is subject to change.

	Mon	Tue	Wed	Thu	Fri
9-9:30					
9:30-10					
10-10:30					
10:30-11					
11-11:30					
11:30-12					
12-12:30			<b>Discussion EGR-1102</b>		<b>Meetings with graduate research assistants</b>
12:30-1					
1-1:30					
1:30-2					
2-2:30		<b>Lecture EGR-3114</b>		<b>Lecture EGR-3114</b>	
2:30-3			Research Meeting		
3-3:30					
3:30-4					
4-4:30					
4:30-5					

## 2. Course Overview

This course provides the electrical & computer engineering student with the analytical and computer skills required for the analysis, computer simulation, design, and computer-aided physical layout of digital integrated circuits. The course is preparatory for study in the field of Very Large Scale Integrated (VLSI) digital circuits and engineering practice.

The objectives of the course are for the student to learn how to model, analyze, simulate, and design digital integrated circuits (CMOS and dynamic logic, for the most part) for engineering applications. By the end of the semester, students should have gained the following skills and/or understanding:

- Basics of (MOSFET) device operation and device physics
- How devices are used to create Boolean logic functions in both CMOS and dynamic logic
- How to build digital systems (e.g., sequential state machines like CPUs)
- How to address some of the issues that arise at high switching speeds
- How to use tools to build (full-custom, semi-custom, and fully synthesized) VLSI circuits and analyze them—tools including Cadence, SPICE, Verilog, and Synopsys

Over the course of the semester, students will have several design projects including rudimentary full-custom structures and slightly more elaborate synthesized structures.

## 3. Course Prerequisite(s)

Students should know digital logic design (ENEE 244), as Boolean logic is the functionality that digital circuits support. Students should also be familiar with basic circuit analysis, as this plays a part in solving some of the difficult problems created by high-speed design techniques.

## 4. Course Material

The required text for the course:

*Digital Integrated Circuits: A Design Perspective, 2nd Ed.*, by Rabaey, Chandrakasan, and Nikolic.

In addition, if you are interested in this topic, I recommend several particularly good texts:

- Dally & Poulton: *Digital Systems Engineering* — this presents an excellent coverage of the issues involved in designing high-speed chips and interfaces.
- Johnson & Graham: *High-Speed Digital Design* — similar to Dally & Poulton, this is an excellent look at the issues in designing high-speed chips and interfaces. Its approach is more practice-oriented than theory-oriented.
- Wolf: *Modern VLSI Design* — this presents an excellent coverage of VLSI issues and manufacturing processes. Similar to the course text, its approach is more practice-oriented than theory-oriented.
- Baker, Li, & Boyce: *CMOS: Circuit Design, Layout, and Simulation* — this is the definitive text on the topic: in-depth, thorough, extremely well done. Also huge.

## 5. Class Projects

Four projects will be assigned during the term, each of which will require a substantial time commitment on your part. You may find the work load in this course to be heavy.

The most common reason for not doing well on projects is not starting them early enough. You will be given plenty of time to complete each project. However, if you wait until the last minute to start, you may not be able to finish. Plan to do some work on a project every day. Also plan to have it finished about 2 days ahead of the due date—many unexpected problems arise during design, especially in the debugging phase. The computing sites can become quite crowded as deadlines approach, making it difficult to get a computer. **Plan** for these things to happen. Your lack of starting early is not an excuse for turning in your project late, even if some unfortunate situations arise such as having your computer crash.

There are many sources of help on which you can draw. Simple questions can be submitted to the TA, professor, and fellow classmates via email (**use the email list given on page 1**). These will typically be answered within the day, often more quickly during working hours. Keep in mind, however, that many types of questions cannot be answered without seeing your project. If you have detailed questions, your best option is to speak to the TA or professor in person during office hours. Bring along a listing of your project, and the output from a run if available. Students are also encouraged to help one another. *One of the best ways for you to make sure that you understand a concept is to explain it to someone else.* Keep in mind, however, that you should not expect anyone else to do any part of your project for you. The project that you turn in must be your own. (*see the following section entitled “Doing Your Own Work”*)

### 5.1 Turning in Projects

Projects are due at 5:00 pm on the due date. We will allow a grace period and accept projects until 11:59 pm. Sometimes unexpected events make it difficult to get a project in on time. For this reason, each person will have a total of 3 free late days to be used for projects throughout the semester. **These late days should only be used to deal with unexpected problems such as computer crashes, illness, or submission problems.** They should not be used simply to start later on a project or because you are having difficulty completing the project. Projects received after the due date (assuming that you have no late days left) will receive a zero, even if it is just one second late. I advise you to save at least one or two late days for the last project. Weekend days are counted in exactly the same way as weekdays (e.g. if the project deadline is Friday and you turn it in Sunday, that's two days late).

### 5.2 Extensions

Extension requests (other than the use of free late days) will be considered only if you ask the professor *before* the original due date. Extensions will only be granted for medical or personal **emergencies**. Be prepared to substantiate any extension request you make with written proof, for example a written note from your doctor. Extensions are not granted for reasons such as: the printer went down, you erased all your files, you lost your program printout, the terminal room was crowded and you couldn't get a terminal, you had other course work or job commitments which interfered, etc. You can avoid all these problems by starting the projects early and keeping backup files. If you are having trouble understanding the material or designing a program, please come to office hours for help right away.

### 5.3 Project Grading

The projects will be graded primarily for correctness (doing all required tasks, simulating at the correct hardware level, and giving correct results). All grading questions should first be discussed with your TA. If you cannot resolve a problem with the TA, bring the project to the instructor.

## 6. Homeworks

Homeworks prepare you for the exams. They will be assigned and collected in the discussion sections. They will be graded on a check/check-minus/check-plus basis. **There will be no late days for homeworks, and homeworks will not be accepted after the beginning of the discussion section.**

## 7. Doing Your Own Work

There are two types of assignments in this class; not surprisingly, we have several different attitudes toward collaboration. In general, all work in this course is to be done on your own. However, at the same time, we want students to help each other learn the course material. As in most courses, there is a boundary separating these two situations. You may give or receive help on any of the topics covered in lecture or discussion and on the specifics of tool operation. You are allowed to consult with other students in the current class during the conceptualization of a project. You are not allowed to use the work or specific ideas of other students. If you have any questions as to what constitutes unacceptable collaboration, please talk to the instructor right away. You are expected to exercise reasonable precautions in protecting your own work; for instance, do not leave a copy of your assignment in a publicly accessible directory, and take care when discarding hardcopy.

### 7.1 Collaboration on Projects

All work on projects is to be your own. Violation will result in a zero on the project or exam in question and initiation of the formal procedures of the Student Honor Council. We will be using an automated program to correlate projects. You may discuss tactics and techniques for solving programming problems, but you are not to stray too far into the details of the solution, else the automated checker might find similarities between different projects. In general, all written work, whether in scrap or final form, must be generated by you working alone. You are not allowed to work out the programming details of the problems with anyone or to collaborate to the extent that your programs are identifiably similar.

### 7.2 Collaboration on Homeworks

In contrast, we highly encourage cooperation on homework assignments, as this is a very effective way for you to learn the material, provided that you think through all the problems. However, if you simply copy someone else's homework, you'll do poorly on the exams, which count five times as much as the homeworks—probably not a good trade-off.

## 8. Exams

You are expected to take both the midterm and final exams at the scheduled times. Unless a (documented) medical or personal emergency is involved in your missing an exam, you will receive a zero for that missed exam. If you anticipate conflicts with the exam time, you must come talk to the instructor about it at least **1 month** before the exam date. The exam dates are given at

the beginning of the term so that you can avoid scheduling job interviews or other commitments on exam days. Outside commitments are not considered a valid reason for missing an exam.

**Exams will be closed book, closed notes.**

## 9. Grading Policy

Final grades will be based on the total of points earned on the projects, homeworks, and exams. The tentative point breakdown is as follows:

Projects: 40%

Homeworks: 10%

Midterm Exam: 20%

Final Exam: 30%

Incompletes will generally **not** be given. According to university policy, doing poorly in a course is not a valid reason for an incomplete. If you are having problems in the course, your best bet is to come talk to the instructor as soon as you are aware of it.

## 10. Tentative Lecture Schedule

Week of	Subject	Readings	Projects
Jan. 22	Course overview	1	
Jan. 29	P/N junctions, MOS transistors	3.1–3.3.2	P1 out
Feb. 5	CMOS Inverter	5.1–5.3	
Feb. 12	Static CMOS design	6–6.2.1	P1 due, P2 out
Feb. 19	Cadence tools, Manufacturing processes		
Feb. 26	Transistor sizing	5.4–5.7	P2 due, P3 out
Mar. 5	Interconnects	4	
Mar. 12	<b>Review &amp; Midterm</b> (Mar. 15, in class)		
Mar. 19	<b>SPRING BREAK</b>		
Mar. 26	Sequential circuits: Latches, registers, pipelines	7	P3 due, P4 out
Apr. 2	Sequential circuits: Latches, registers, pipelines	7	
Apr. 9	Capacitive, resistive, and inductive parasitics	9	
Apr. 16	System timing: Synchronous, asynchronous, etc.	10	P4 due, P5 out
Apr. 23	System timing: Synchronous, asynchronous, etc.	10	
Apr. 30	Memories: SRAM circuits	12	
May 7	Memories: DRAM systems & circuits	<i>not really in book</i>	P5 due
Exams	<b>Exam</b> (Wed May 16, 10:30am)		

## 11. Special Needs

If you have a documented disability that requires special needs, please see me as soon as possible, and certainly no later than the third week of classes.