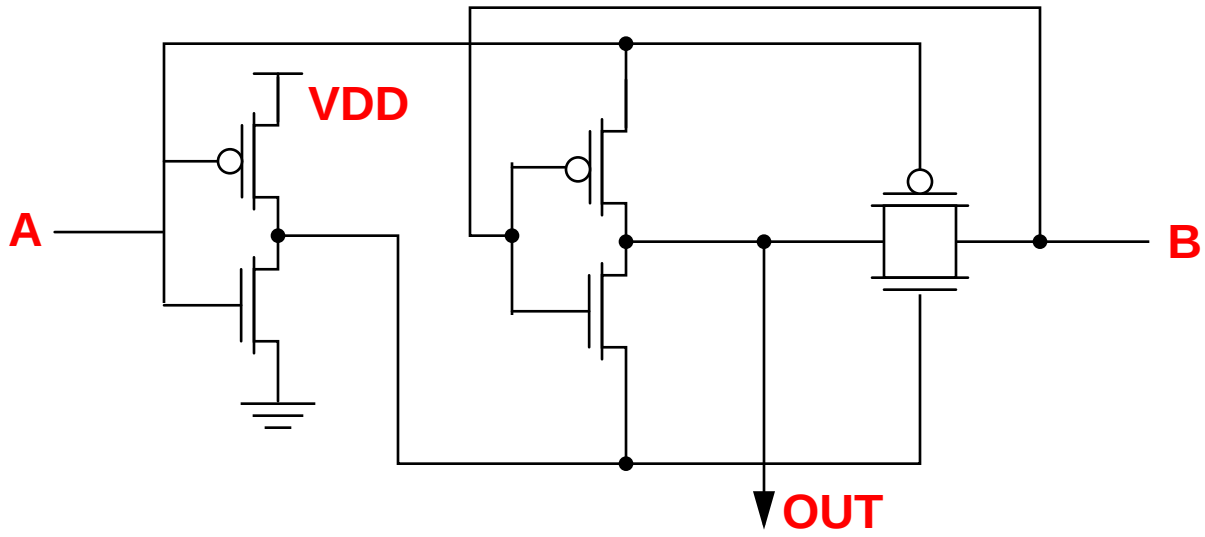
Homework 4

ENEE 359a: Digital VLSI Design, Spring 2007

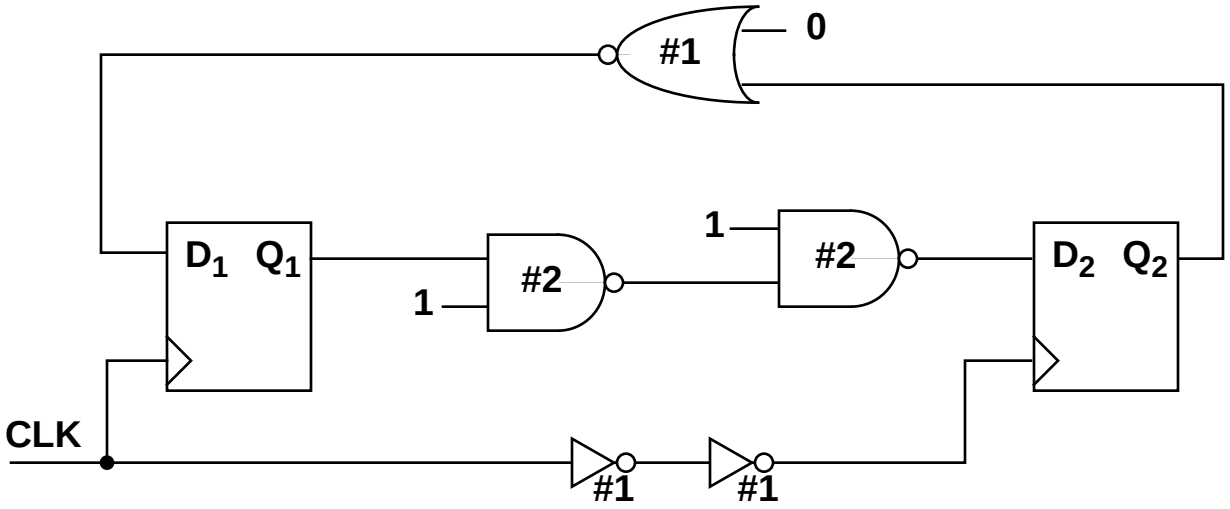
1. Transmission Gate Logic

What is the output function of the following circuit?

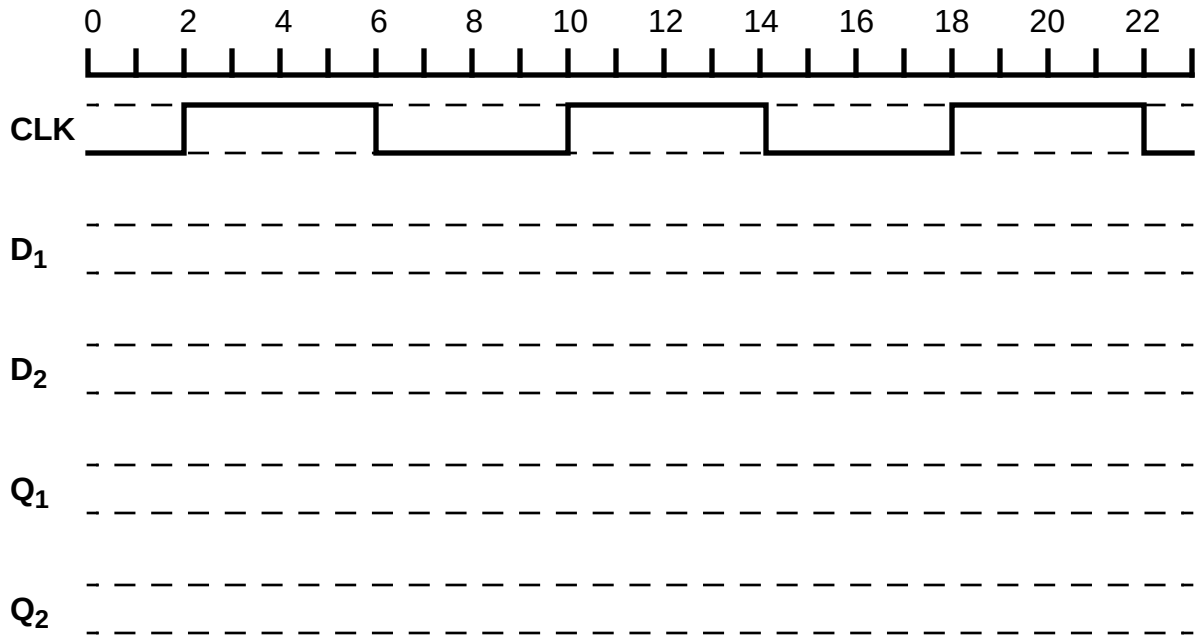


2. Pipelines I: Timing

The circuit shown below uses two identical rising edge triggered Flip-Flops. Assume that for both Flip-Flops, the *setup time* is one time unit, the *propagation delay* is one time unit, and the *hold time* is two time units. The gates, buffers and inverters in this circuit are annotated with their propagation delays in the same time units. Assume that maximum and minimum propagation delays for these gates are equivalent.



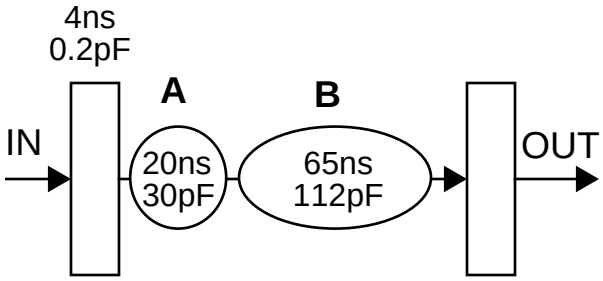
A. Complete the following timing diagram for the circuit. Assume the initial states of Q_1 and Q_2 are 0, and have remained at 0 for a long time (but no clock edge has come along yet to latch the 1 value at D_1).

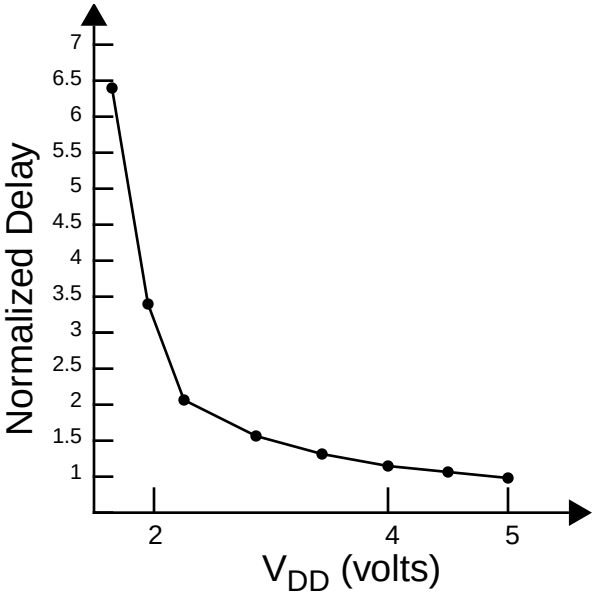


B. What is the *minimum clock period* of this circuit that will assure that it works? Describe the critical path.

3. Pipelines II: Power

Consider the circuit below, left. Modules A and B have a delay of 20nsec and 65nsec at 5V and switch 30pF and 112pF, respectively. Each register has a delay of 4nsec and switches 0.2pF. Adding a pipeline register between A and B allows for reduction of the supply voltage while maintaining the throughput. How much power can be saved this way? (Delay with respect to VDD can be approximated from the plot on the right.)





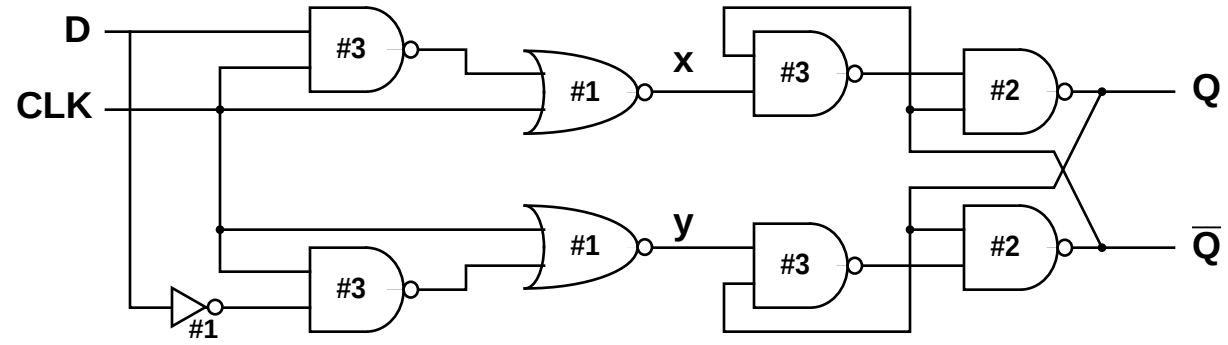
4. Flip-FLop Timing

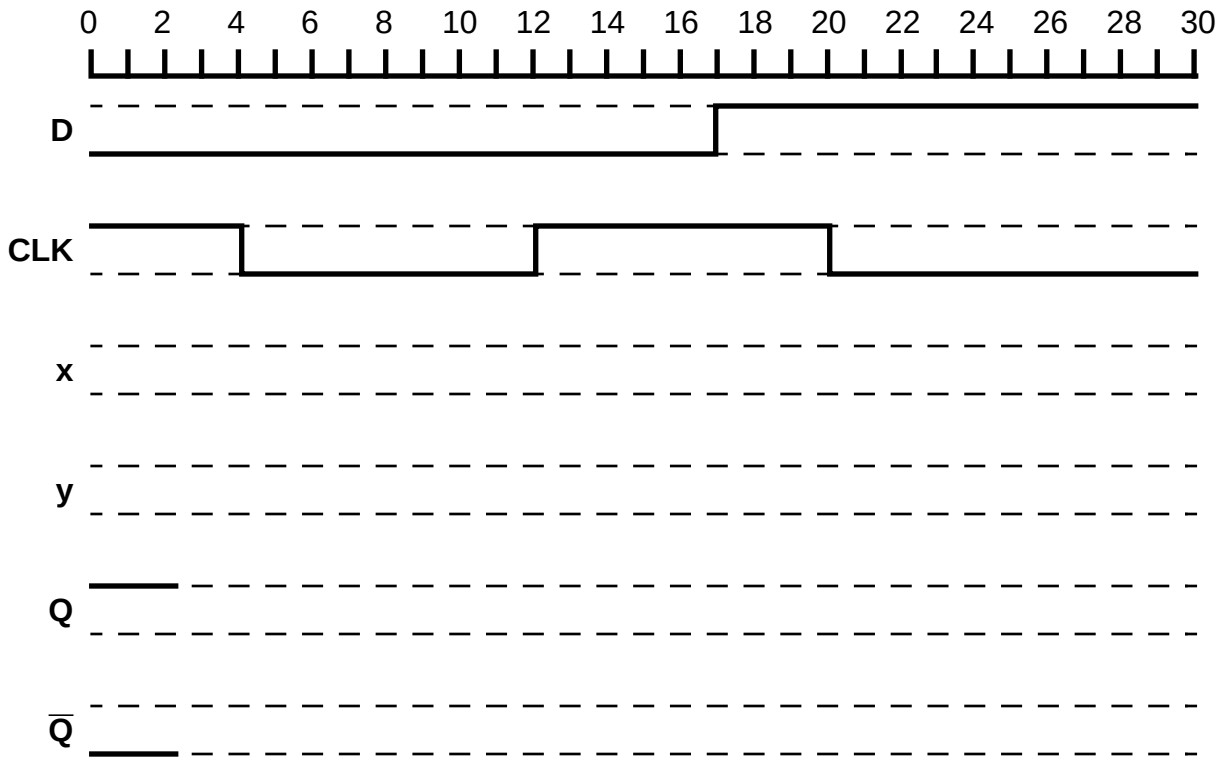
In the flip-flop below, the gates are annotated with their delay in time units. Assume the initial state of the flip-flop is Q = 1, $\overline{Q}$ = 0.

A. Fill out the timing diagram to illustrate the behavior of the circuit.

B. Determine the worst-case Clock-to-Q propagation time.

C. Determine the worst-case set-up (D-to-Clk) time.





5. Elmore Delay

Using the Elmore-delay model, compute the RC delay from the source node (node 0) to sink nodes 1 through 5.