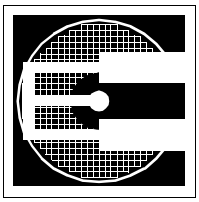


Midterm Exam (20%)

ENEE 359a: Digital VLSI Design
March 13, 2008

This exam should take you less than an hour: 5 questions, 10 minutes apiece. The exam is closed book, closed notes.

Note that each question is worth the same number of points; this means you should do those questions you find easy first.

Solutions

Name: _____

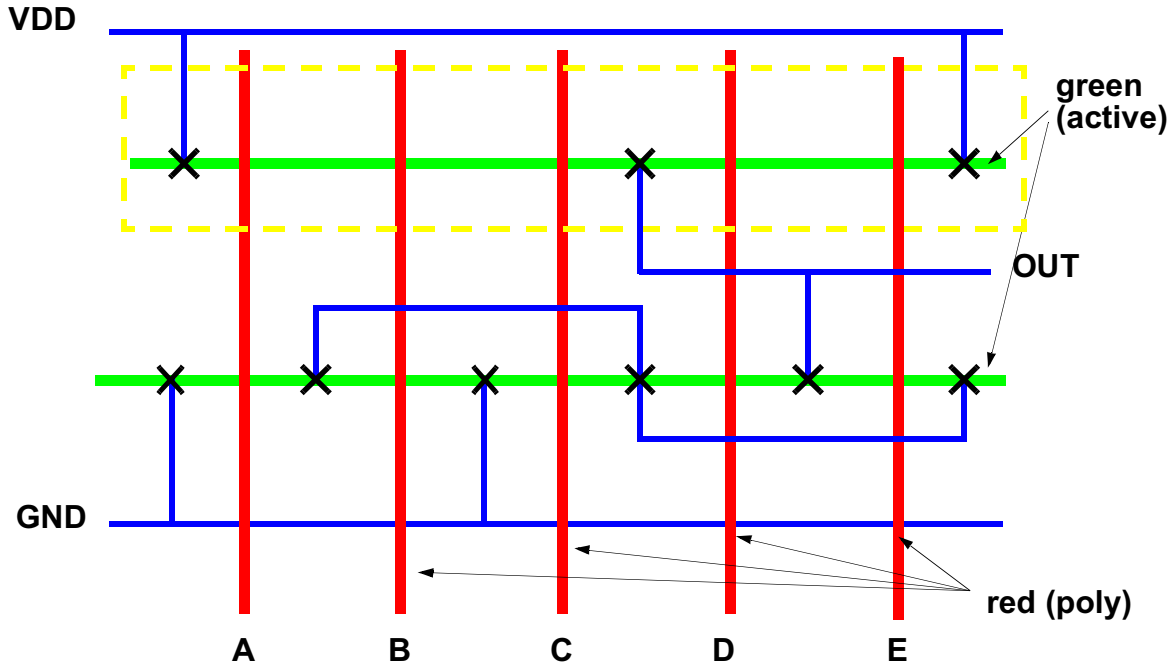
Score:

Problem 1:	out of 4
Problem 2:	out of 4
Problem 3:	out of 4
Problem 4:	out of 4
Problem 5:	out of 4
Total:	

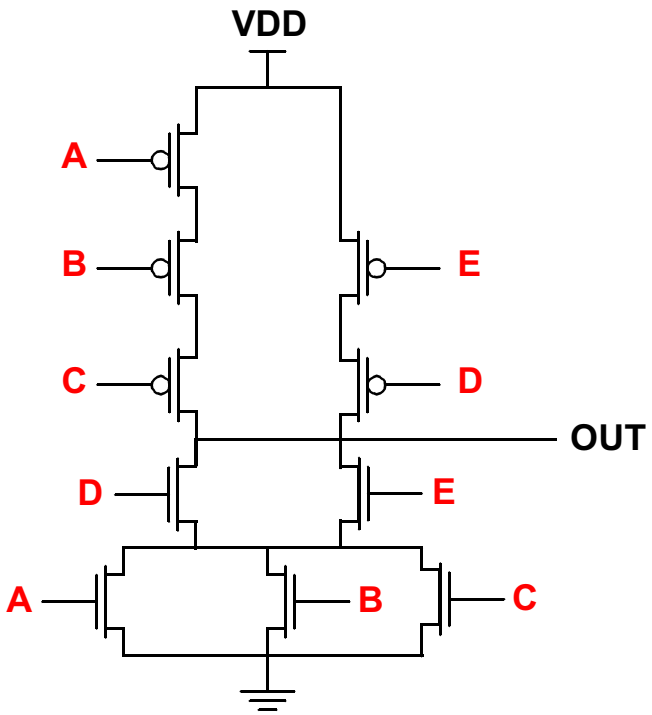
Grade Distribution:

19 - X
18 - X X
17 - X X X
16 - X
15 - X X

1. **Consider the following stick diagram. Draw the electrically equivalent transistor-level schematic. What logic equation does the circuit implement?**



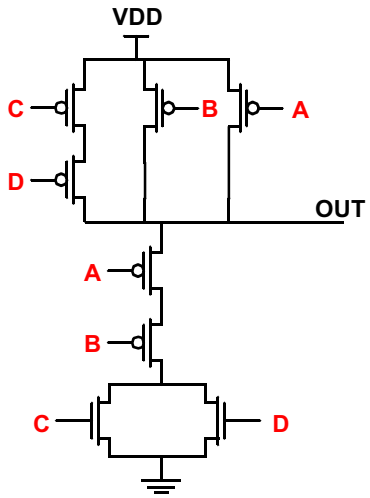
solution:

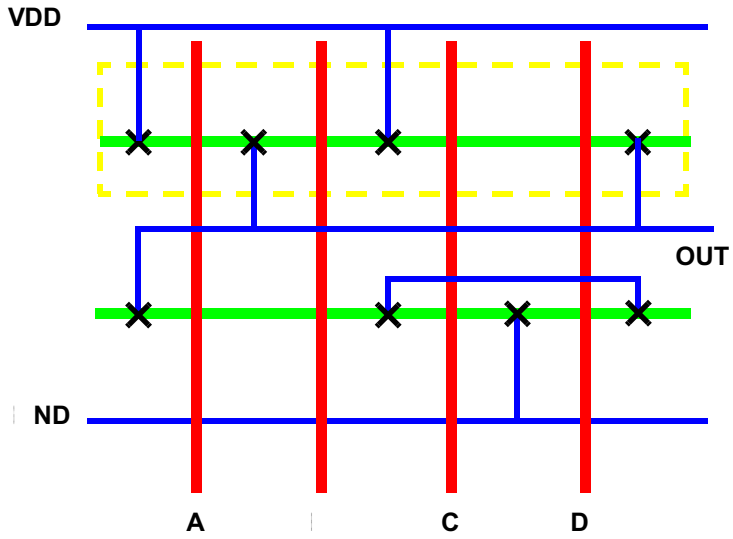


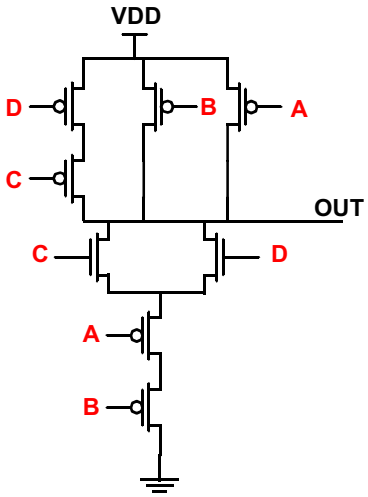
$$out = \sim((A+B+C)(D + E))$$

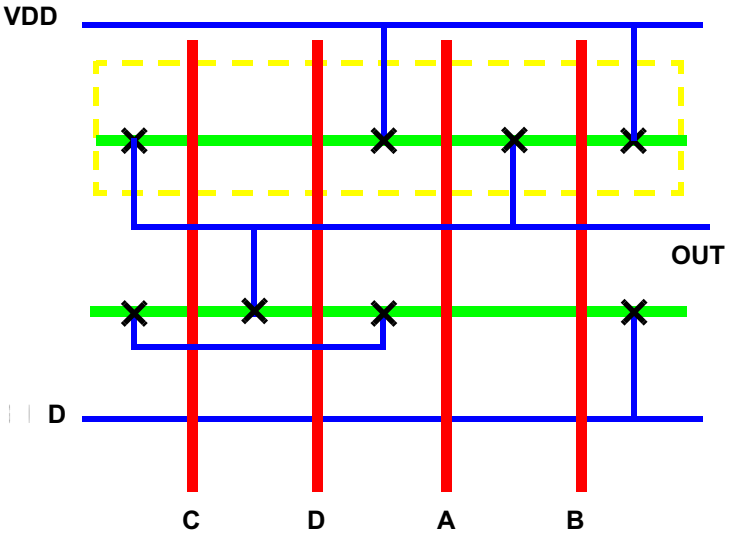
2. Consider the logical expression out = ~(ab(c+d))**. Convert this to a schematic diagram for static CMOS logic, then convert it to a stick-diagram layout (as in question 1).**

some equivalent solutions (there is way more than one correct answer):

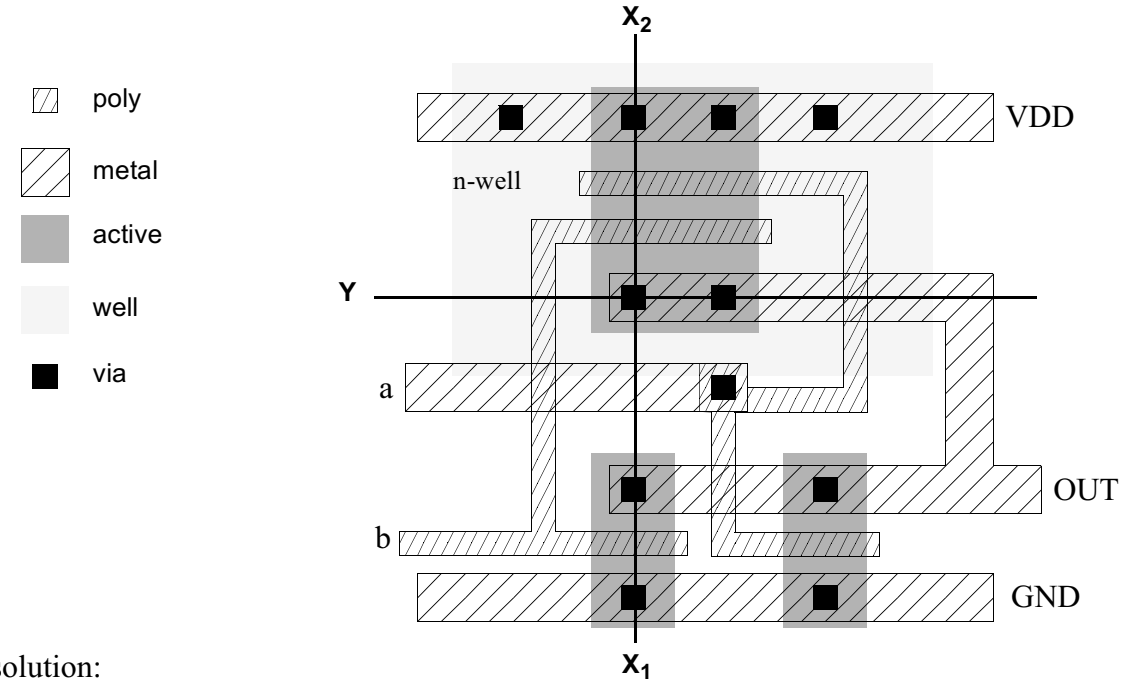




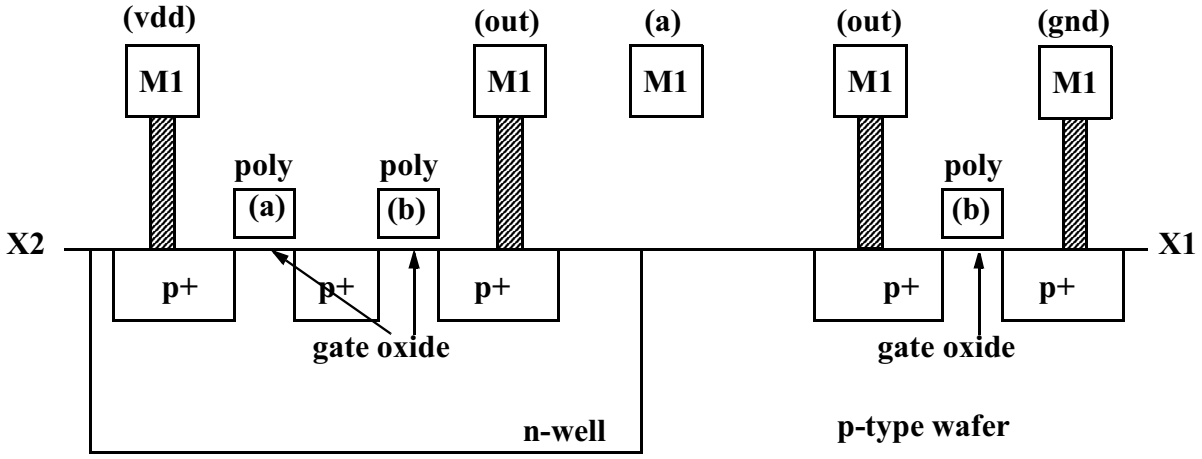


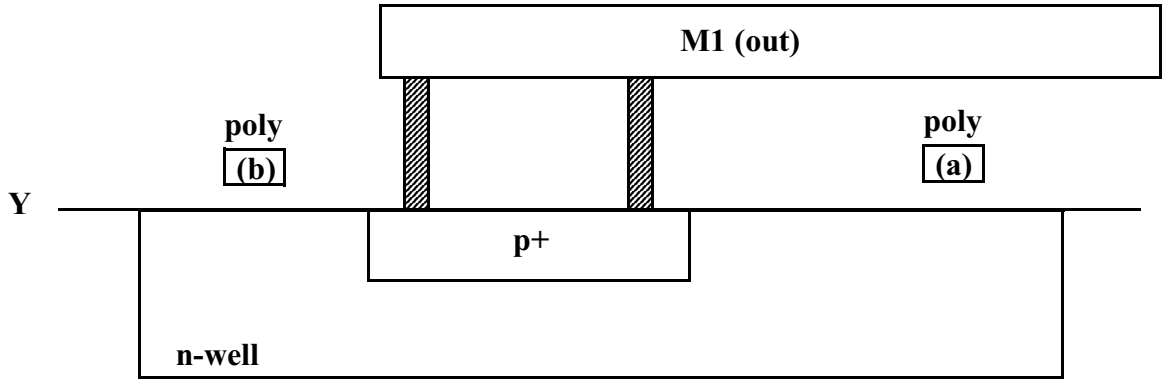


3. Provide a side-view diagram for each of the cuts X and Y through the layout below. Be sure to label each of the strata. Label your endpoints for the X cut, so it is clear which end is which.



solution:



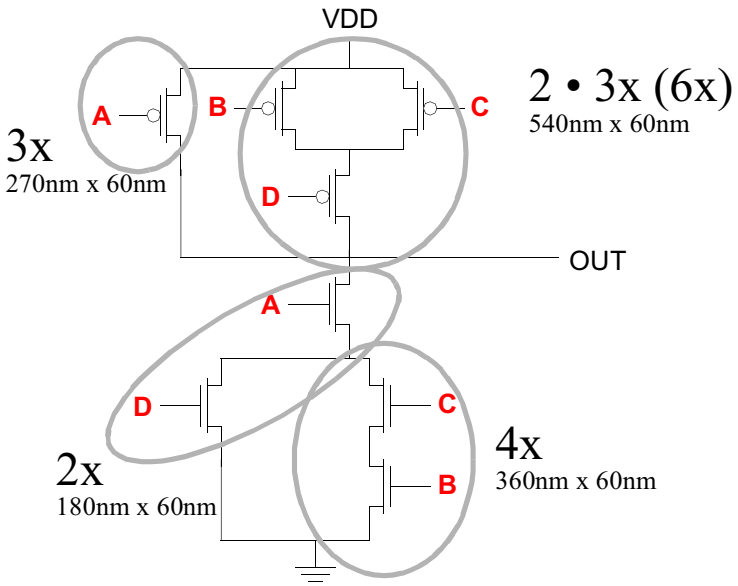


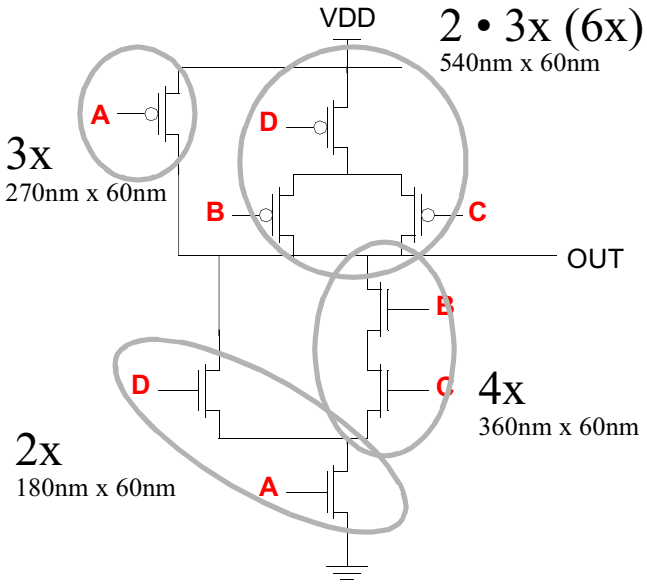
4. **Consider the function** out = ~(a • (bc + d)). **Draw the circuit and size the transistors: size all NMOS and PMOS transistors so that the PUN and PDN each has equivalent resistance to a minimum-sized MOSFET, and then take into account the fact that $\mu_n = r \cdot \mu_p$ where $r = 3$ (i.e. the resistance of a unit PMOS device is 3 times that of a unit NMOS device).**

Important: Assume the circuit is implemented in a 60nm technology and that the dimensions of a **minimum-sized MOSFET** in this technology are **90nm width x 60nm length**. Express the dimensions of each MOSFET in the optimized circuit in nanometers (W nm x L nm).
I.e., what is it that you are scaling?

some equivalent solutions (there is more than one correct answer):

min. device: WxL = 90nm x 60nm





5. Choose *one* of the following two essay questions and answer it.
Do not write more than two pages. Diagrams are always helpful.

A. Explain the behavior of a p/n junction under equilibrium, forward-bias, and reverse-bias scenarios.

B. How does an n-type MOSFET work? Why does the current saturate at high V_{DB}?