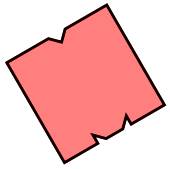
ENEE 359a
Digital VLSI Design

Static CMOS Logic

Prof. Bruce Jacob

blj@eng.umd.edu

Credit where credit is due:
Slides contain original artwork (© Jacob 2004) as well as material taken liberally from Irwin & Vijay's CSE477 slides (PSU), Schmit & Strojwas's 18-322 slides (CMU), Wolf's slides for *Modern VLSI Design*, and/or Rabaey's slides (UCB).

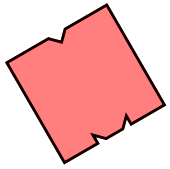


Bruce Jacob

University of Maryland
ECE Dept.

Overview

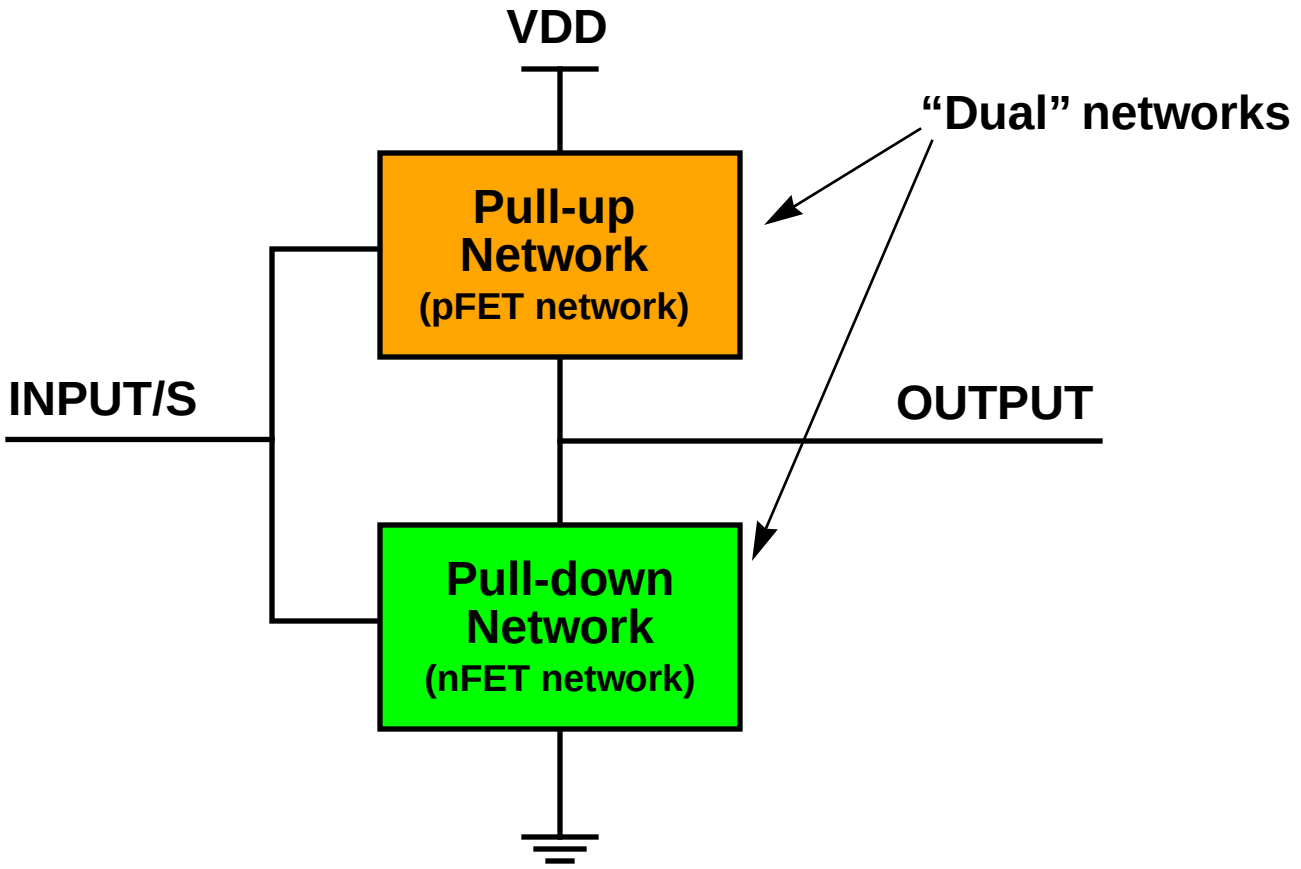
- **General complementary logic design, perspective, stick-figure circuit diagrams**
- **Examples: constructing PDN/PUN duals, logic -> circuit, circuit -> logic, circuit -> layout, layout -> circuit, cross sectional views of layout**



Bruce Jacob

University of
Maryland
ECE Dept.

Complementary Design

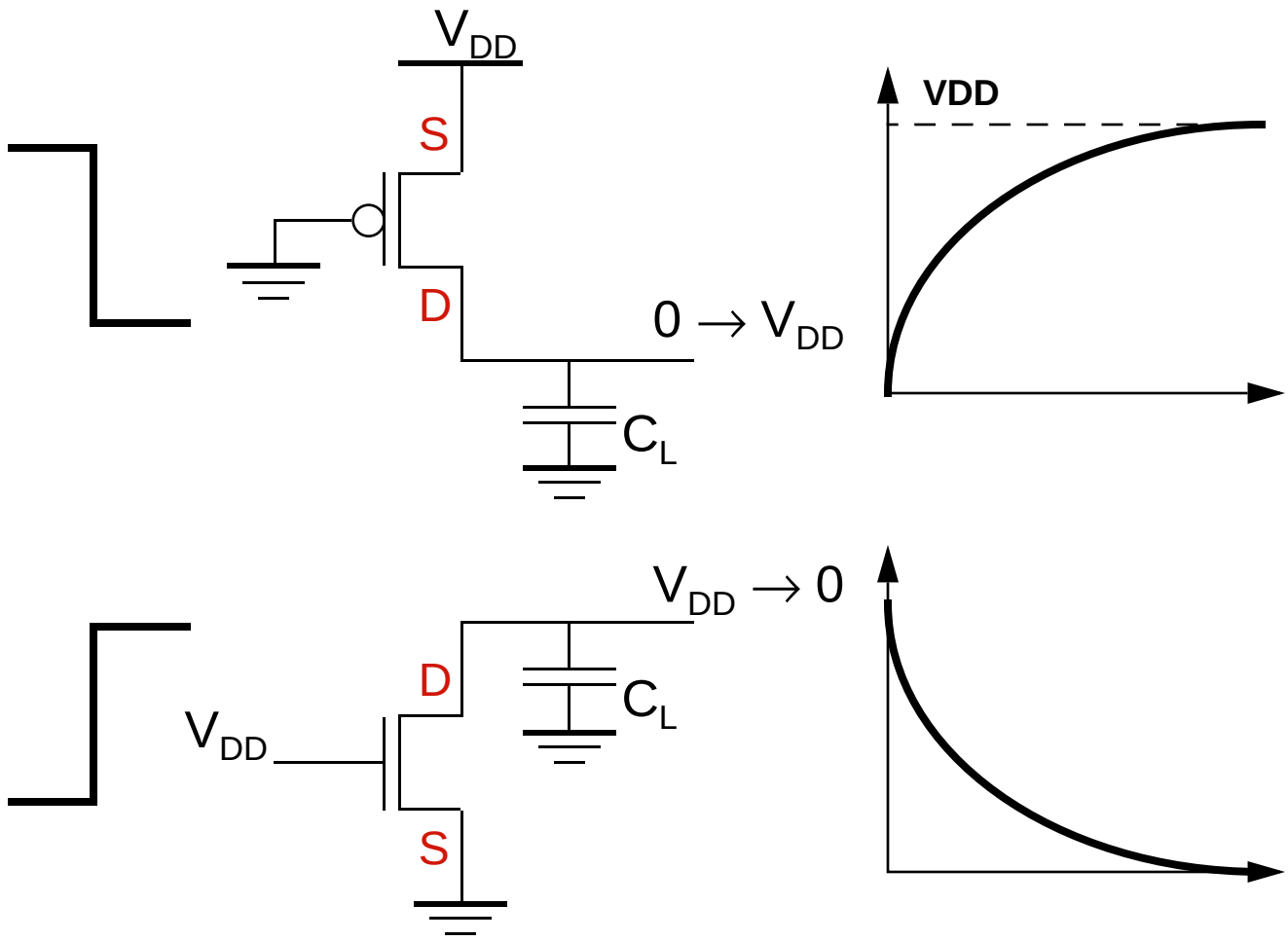


- PMOS "Pull-Up" Network (PUN)
- NMOS "Pull-Down" Network (PDN)

Bruce Jacob

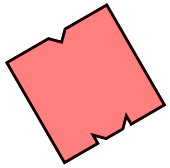
University of
Maryland
ECE Dept.

Why Division?



PMOS will pass a “1”

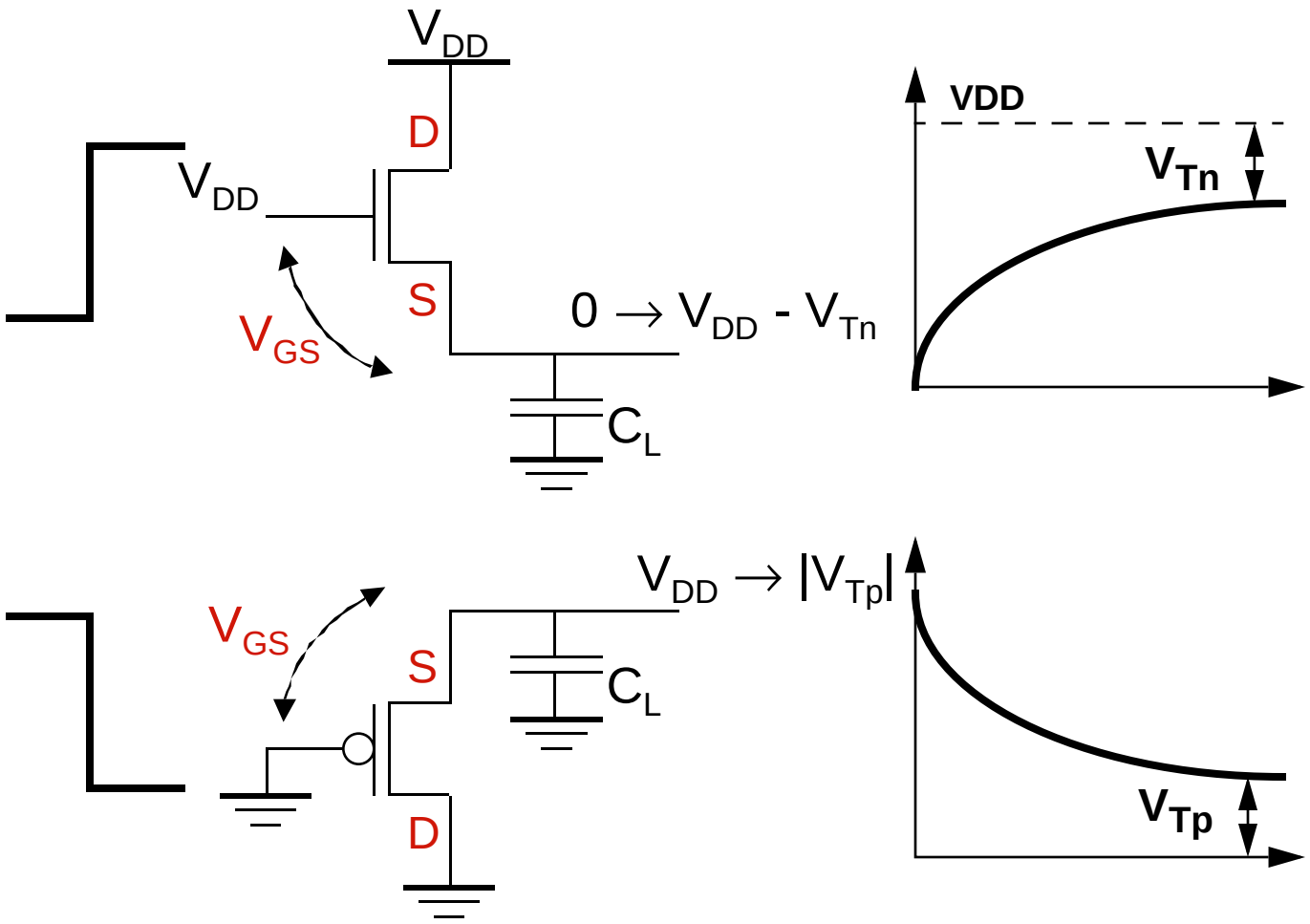
NMOS will pass a “0”



Bruce Jacob

University of
Maryland
ECE Dept.

Why Division?



NMOS will not pass a “1”

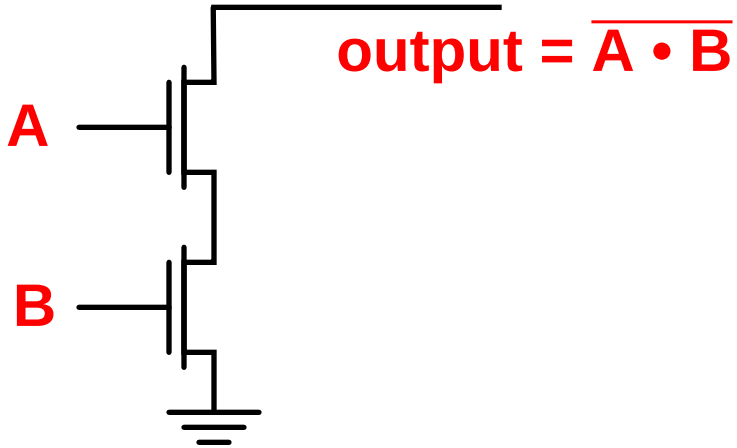
PMOS will not pass a “0”

Bruce Jacob

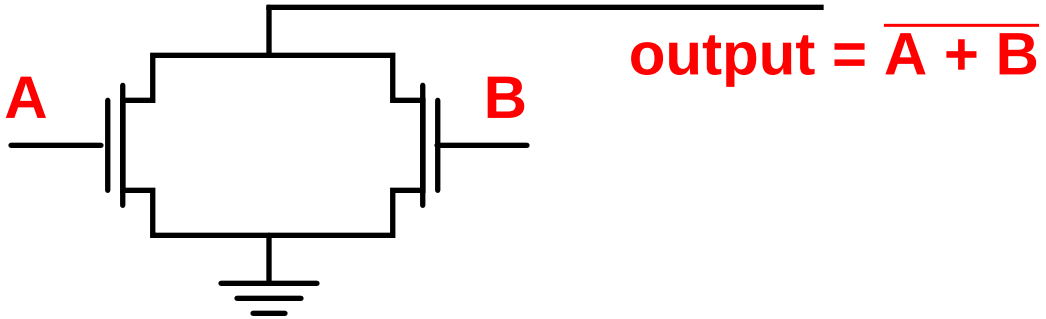
University of
Maryland
ECE Dept.

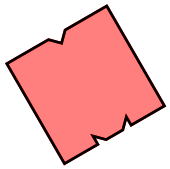
Building Blocks

NMOS devices in series
implement a NAND function



NMOS devices in parallel
implement a NOR function

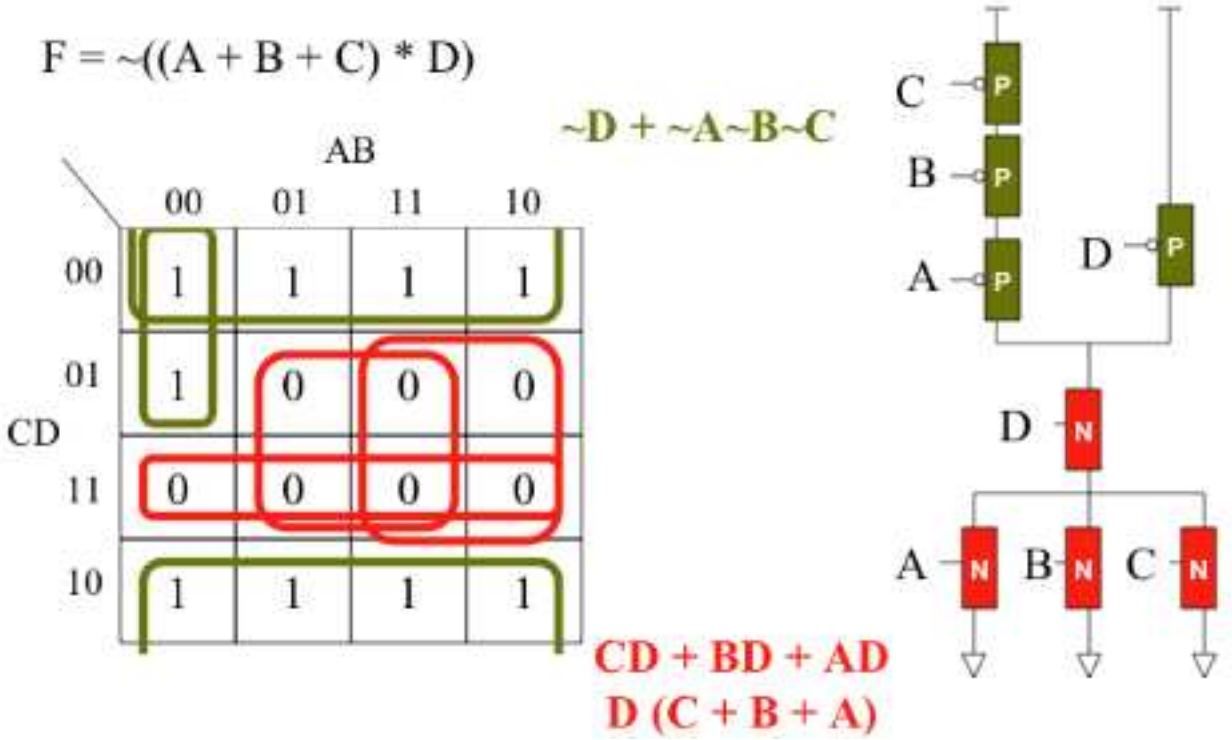




Bruce Jacob

University of
Maryland
ECE Dept.

Implements Arbitrary Logic



- **Pull-Up Network: on when function = 1**
- **Pull-Down Network: on when function = 0**

Static CMOS: Perspective

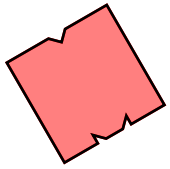
- **"Static" as in "output is logic function of inputs, and, given stable inputs, it does not change over time"**
- **Propagation delay function of load capacitance and resistance of transistors**

PROS:

- **Full rail-to-rail swing; high noise margins**
- **Logic levels not dependent upon relative device sizes**
- **Always a path to Vdd or Gnd in steady state; low output impedance**
- **Extremely high input resistance; nearly zero steady-state input current**
- **No direct path steady state between power and ground; no static power dissipation**

CONS:

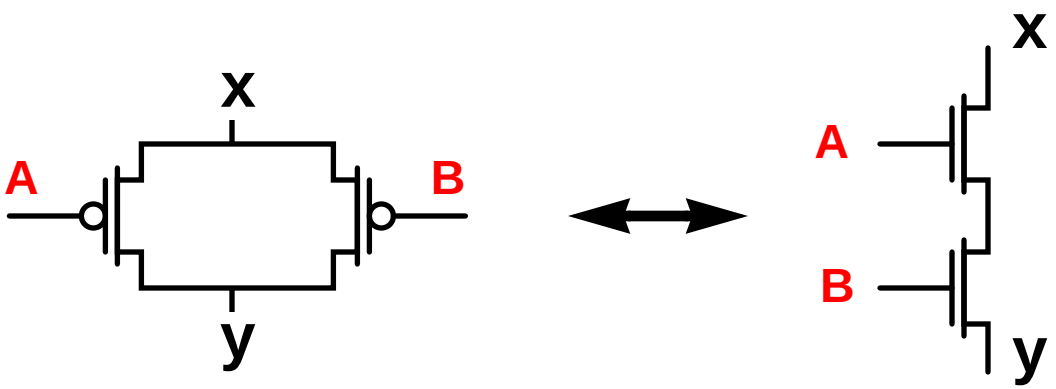
- **N inputs => 2N transistors in design**



Bruce Jacob

University of
Maryland
ECE Dept.

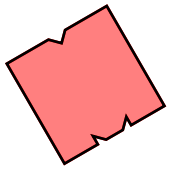
Constructing the Dual



Transistors in parallel are in series in dual; transistors in series are in parallel in dual

This is the physical realization of DeMorgan's theorems:

- $\overline{A + B} = \overline{A} \bullet \overline{B}$ **[!(A + B) = !A • !B *or* !(A | B) = !A & !B]**
- $\overline{A \bullet B} = \overline{A} + \overline{B}$ **[!(A • B) = !A + !B *or* !(A & B) = !A | !B]**

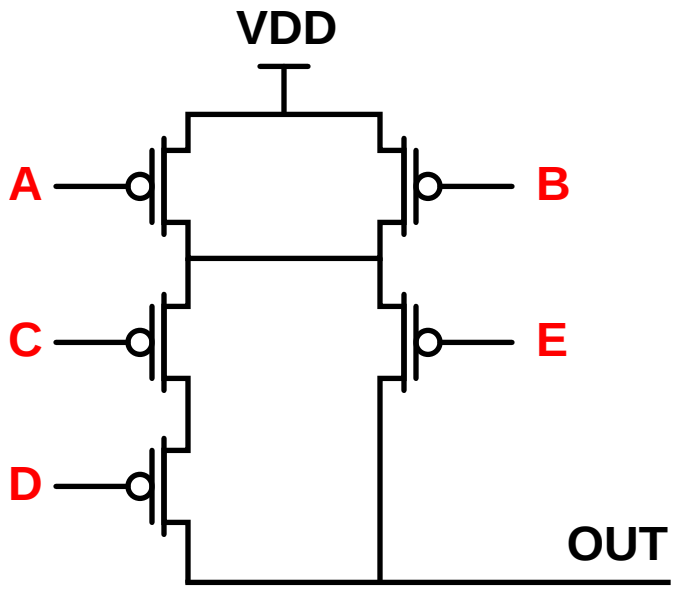


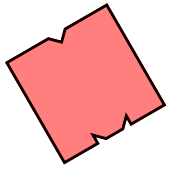
Bruce Jacob

University of
Maryland
ECE Dept.

Examples

Constructing the Dual



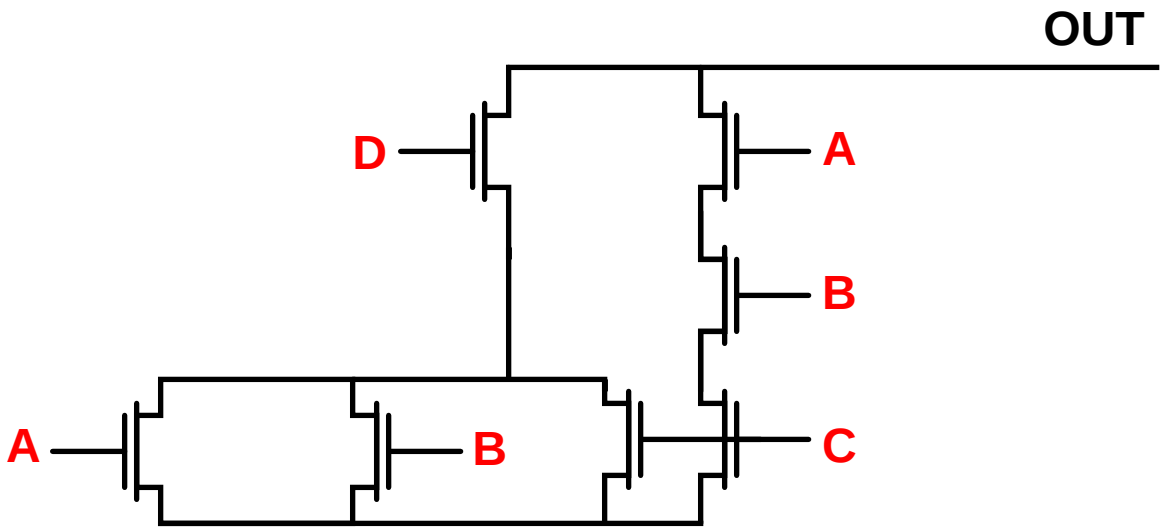


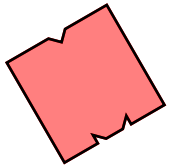
Bruce Jacob

University of
Maryland
ECE Dept.

Examples

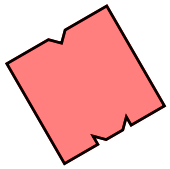
Constructing the Dual





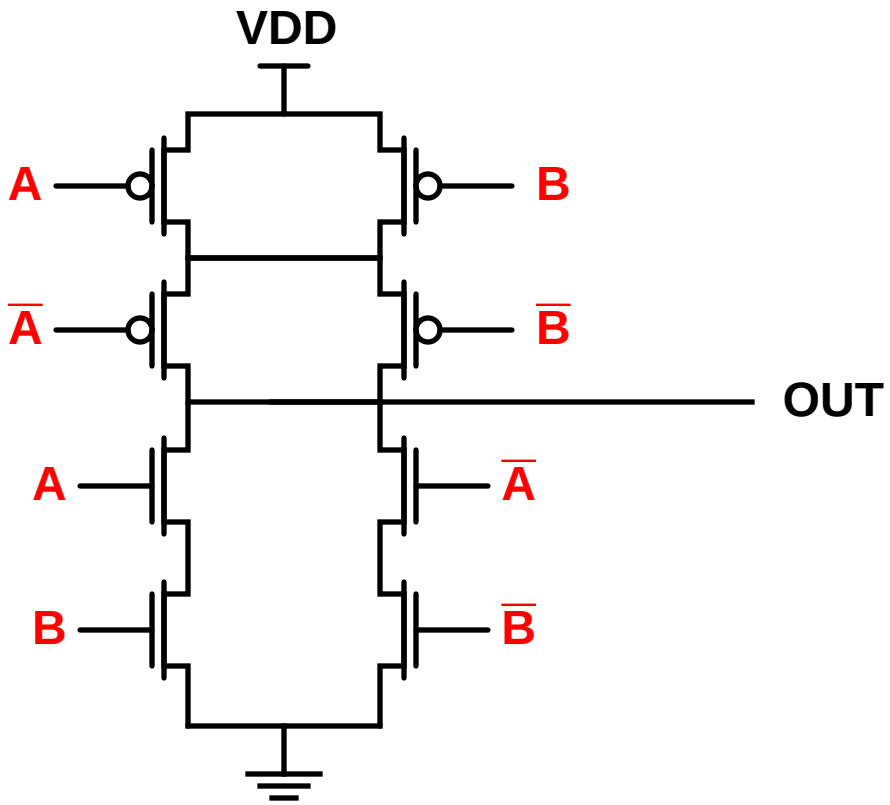
Examples: Logic <-> Circuit

- **XOR [out = ~($\overline{A}$ $\overline{B}$ + A B)]**



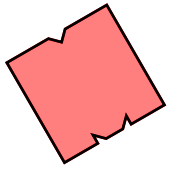
Examples: Logic <-> Circuit

- **XOR [out = ~($\overline{A}$ $\overline{B}$ + A B)]**



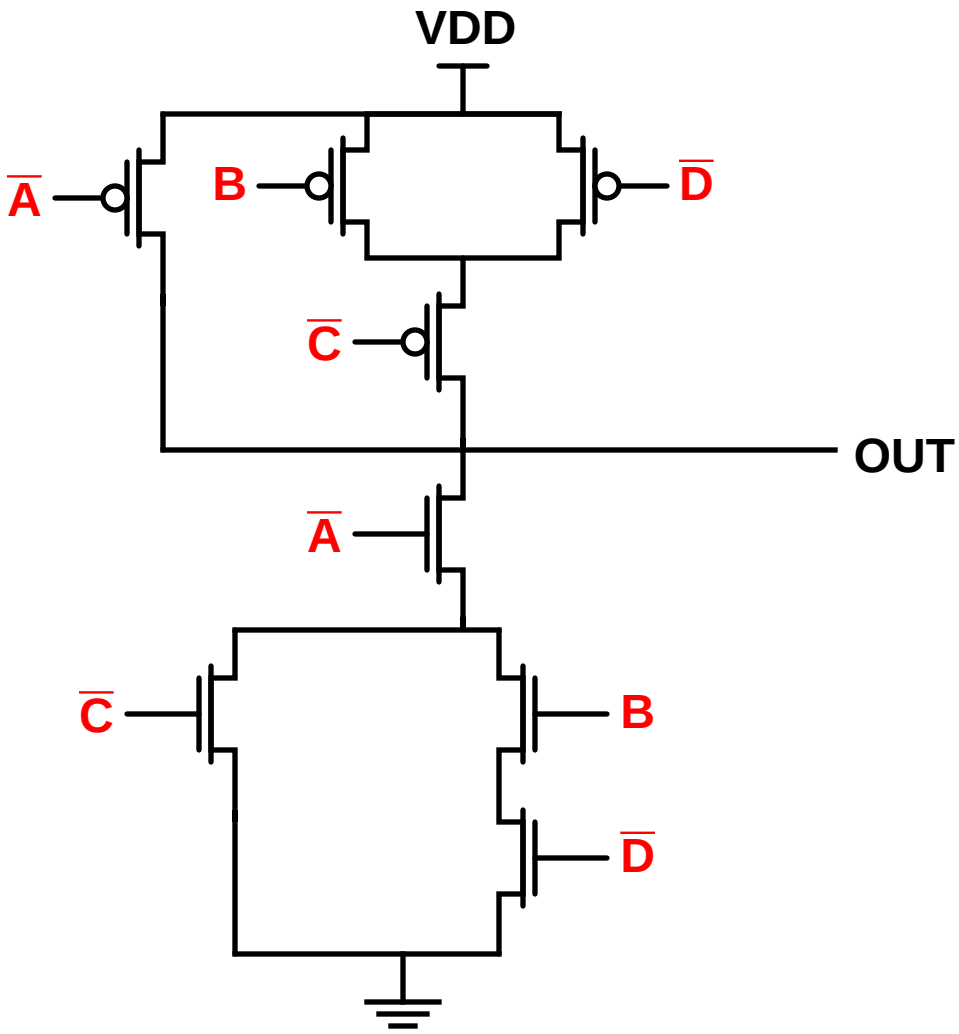
Examples: Logic <-> Circuit

- **out = ~($\overline{A}$ • ($\overline{C}$ + B$\overline{D}$))**



Examples: Logic <-> Circuit

- **out = ~($\overline{A}$ • ($\overline{C}$ + B$\overline{D}$))**



Bruce Jacob

University of
Maryland
ECE Dept.

SCMOS

SCALABLE DESIGN RULES

CMOS Scales Well … Exploit That Fact

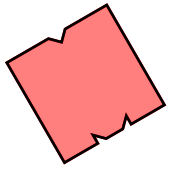
- Implement it now, shrink it later
- Express all design rules in terms of unit dimension
- Change dimension of the unit, whole design shrinks
- Mead & Conway

Unit Dimension: Minimum Line Width (2λ)

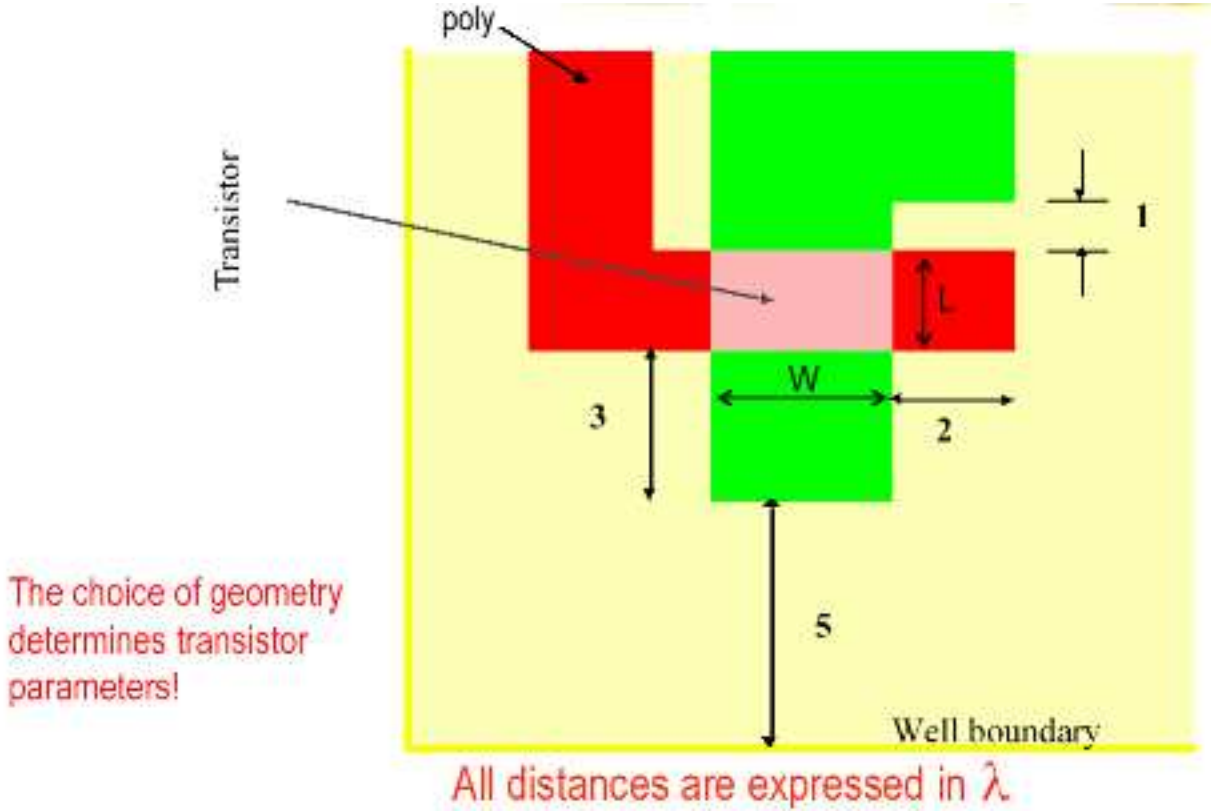
- In 1978, λ = 1.5 µm (a.k.a. 3 micron technology)
- In 2004, λ = 0.045 µm (a.k.a. 90 nanometer technology)

Important Intellectual Idea
(but not used in industry) (but we will)

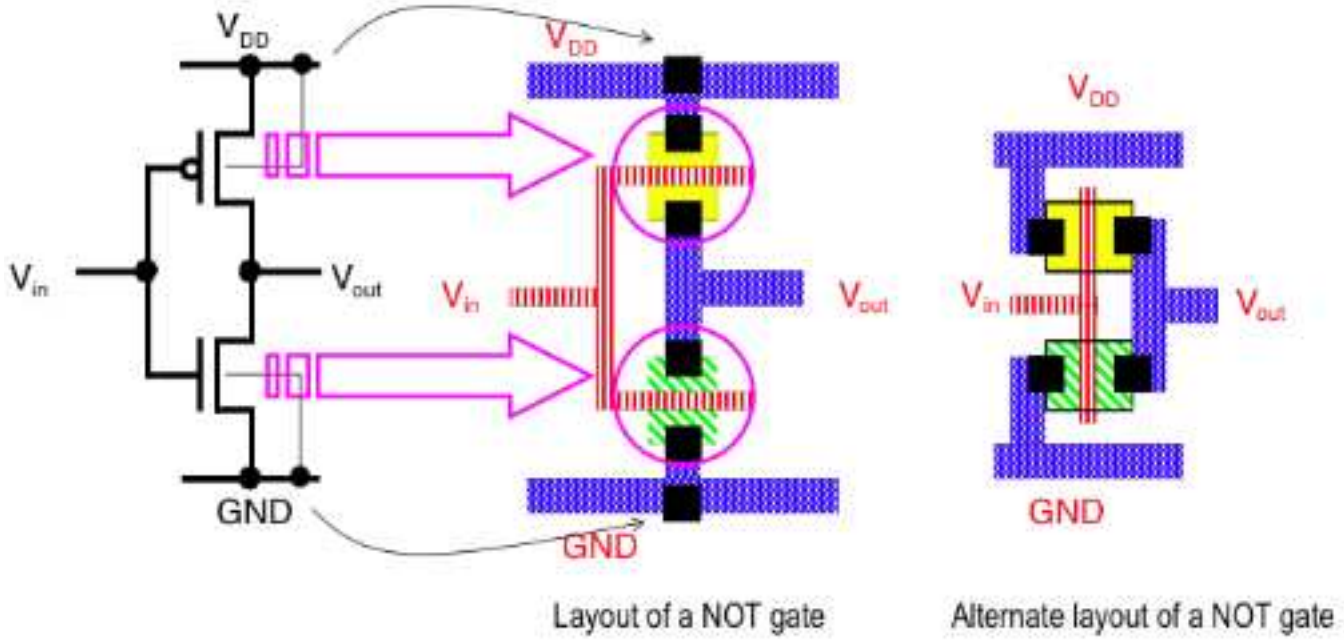
(why not? elegance costs $$$ … currently *thousands* of design rules)



How lambda is used ...



Layout <-> Circuit



Layout of a NOT gate

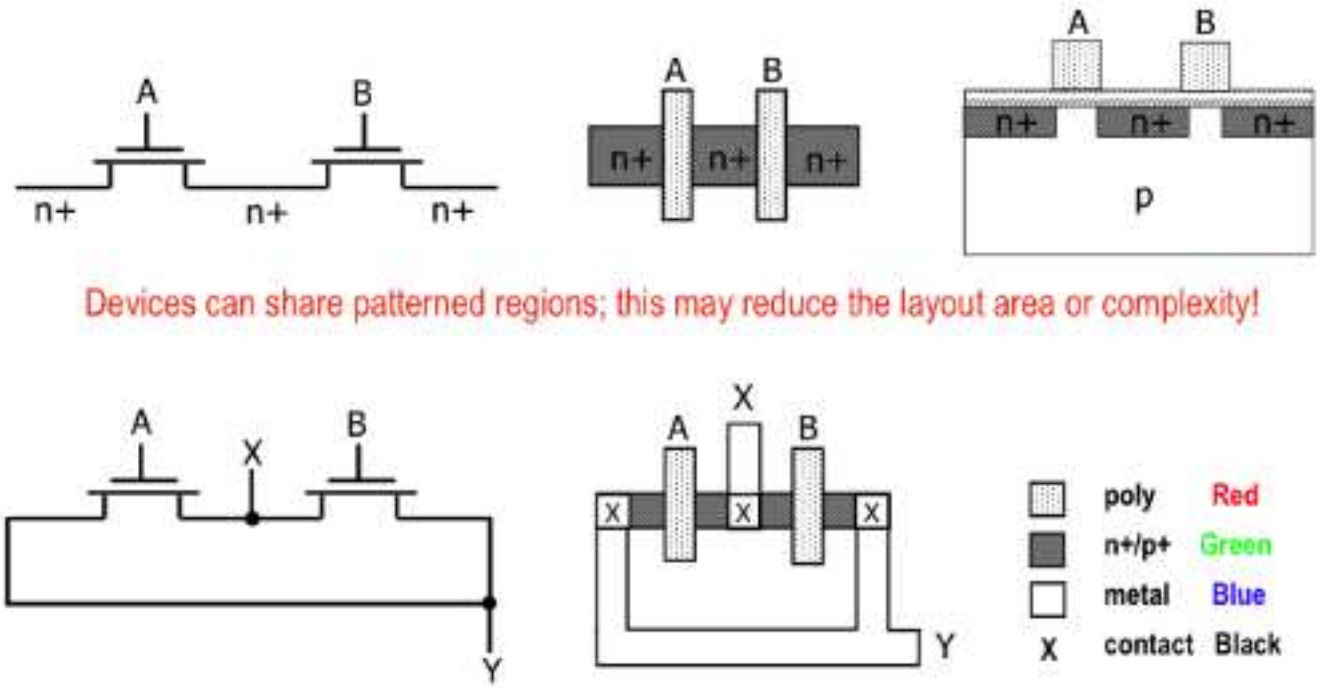
Alternate layout of a NOT gate

magenta		**Metal 2**
blue		**Metal 1**
red		**Polysilicon (gate material)**
green		**Active area (n+ or p+ diffusion)**
yellow		**Well (p or n)**
black		**Contact (via)**

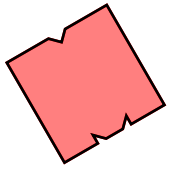
Bruce Jacob

University of
Maryland
ECE Dept.

Layout <-> Circuit

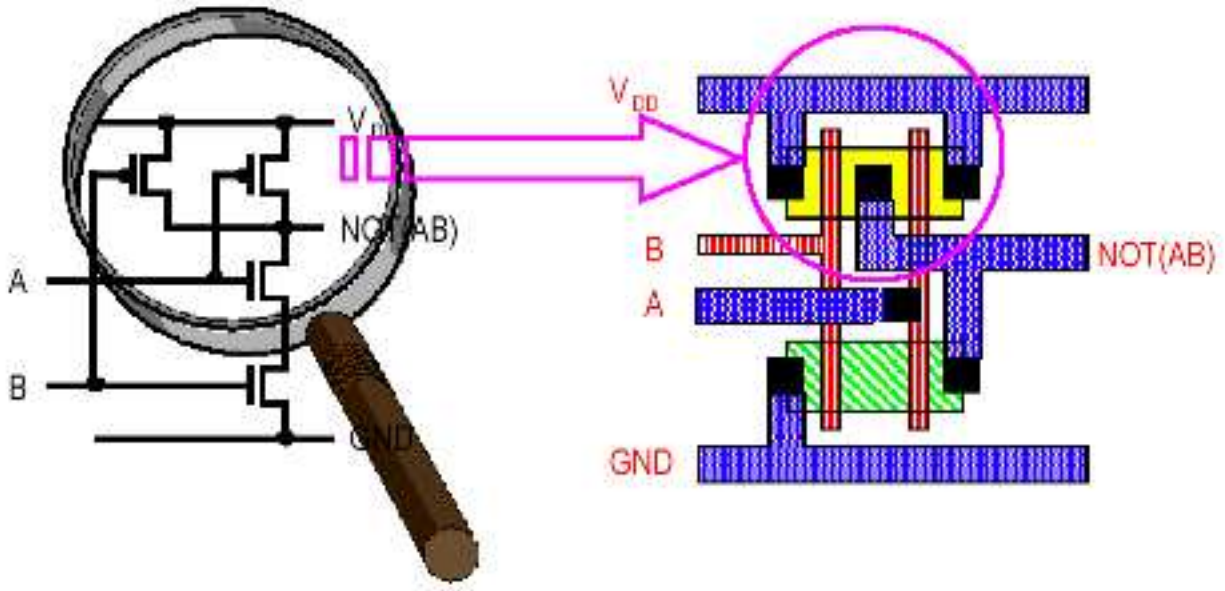


- **FETs in series: source-drain overlap**
- **FETs in parallel: can share source/drain**



Layout <-> Circuit

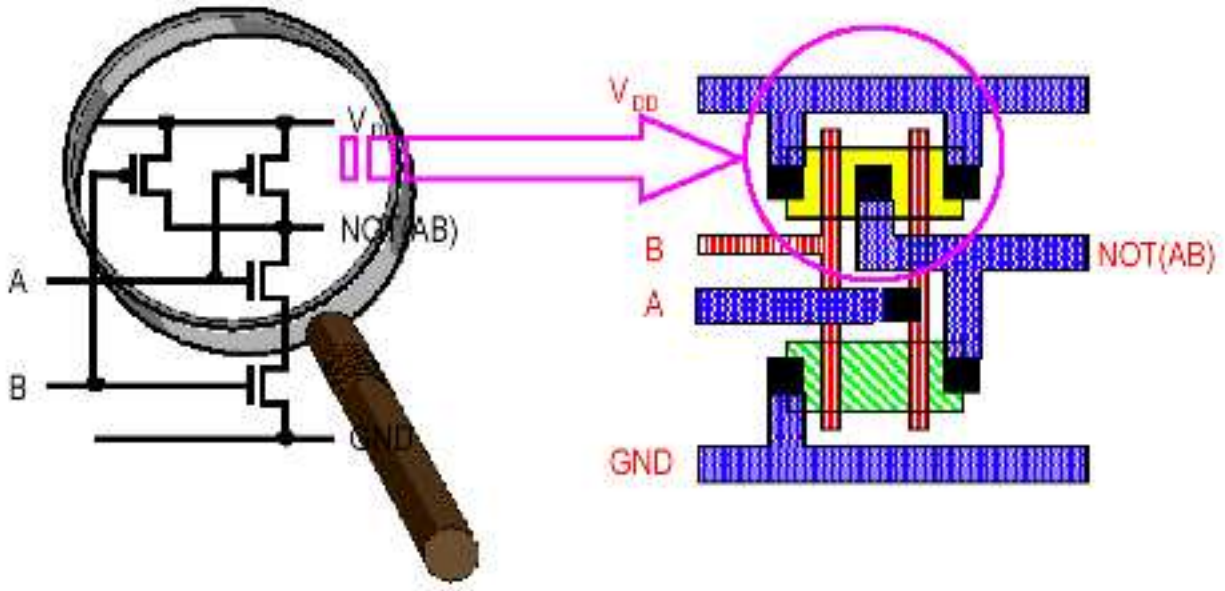
2-INPUT NAND



- **FETs in series (in NAND PDN): source-drain overlap**
- **FETs in parallel (in NAND PUN): share drain**

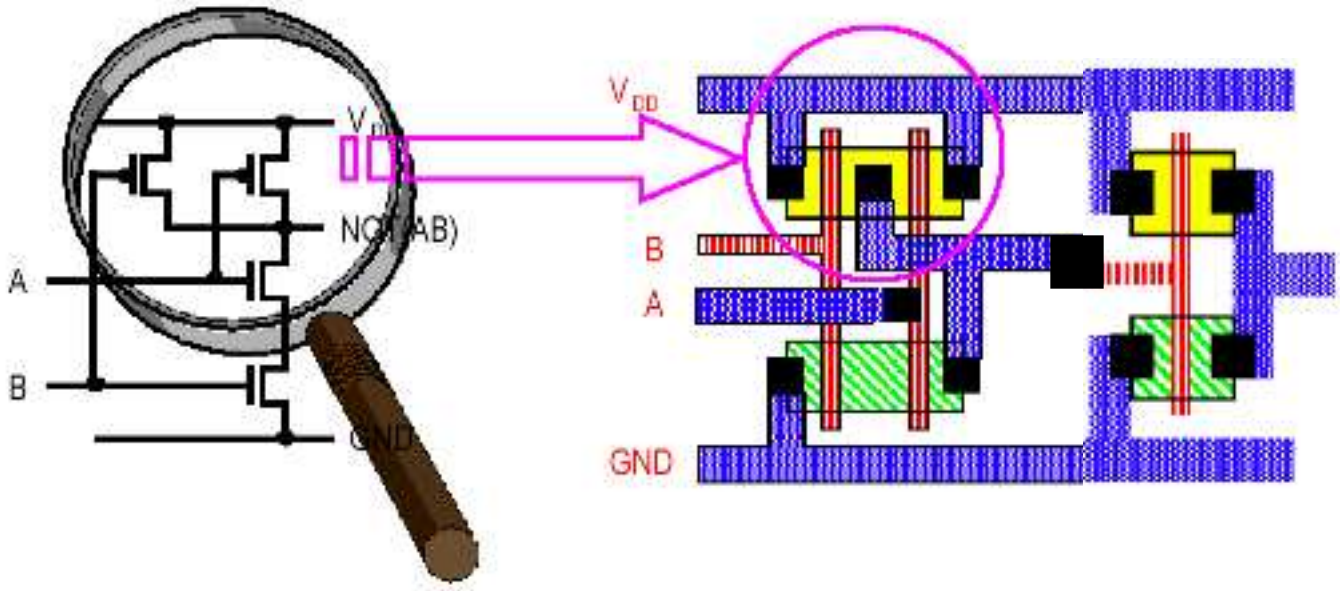
Layout <-> Circuit

How About 2-INPUT AND?



Layout <-> Circuit

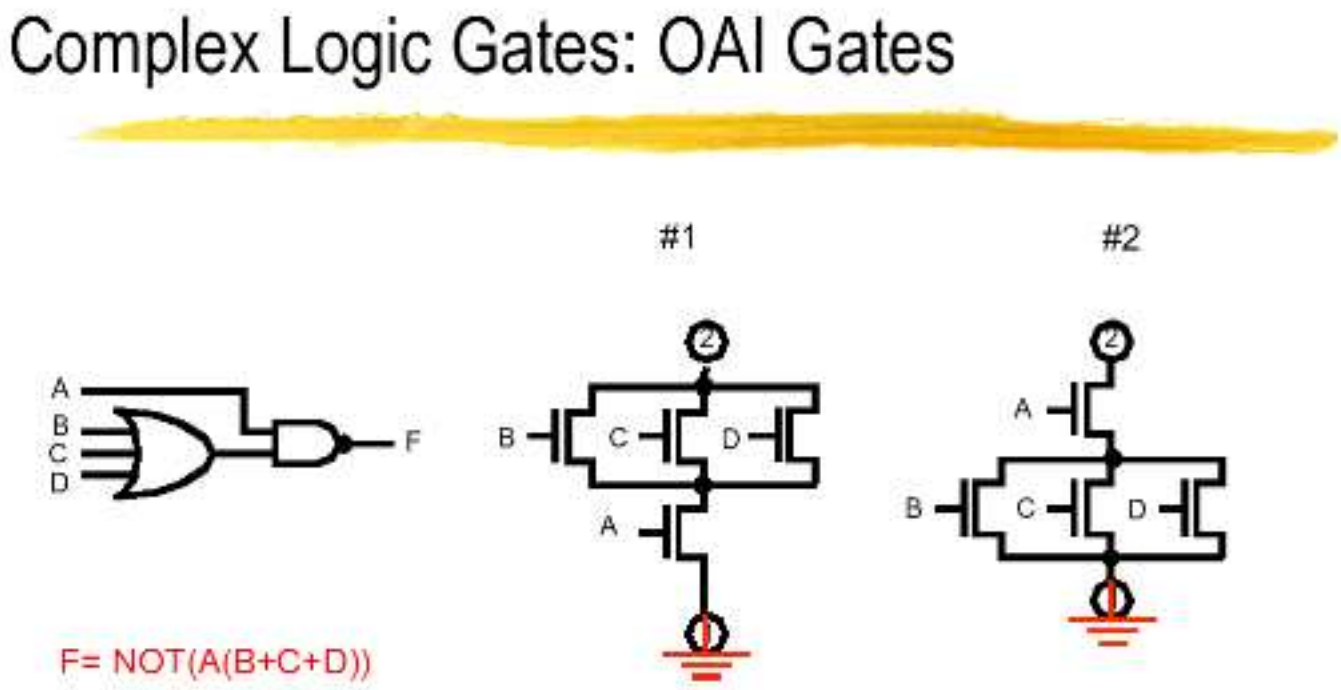
How About 2-INPUT AND?



Add an inverter at the end …

Examples: Layout <-> Circuit

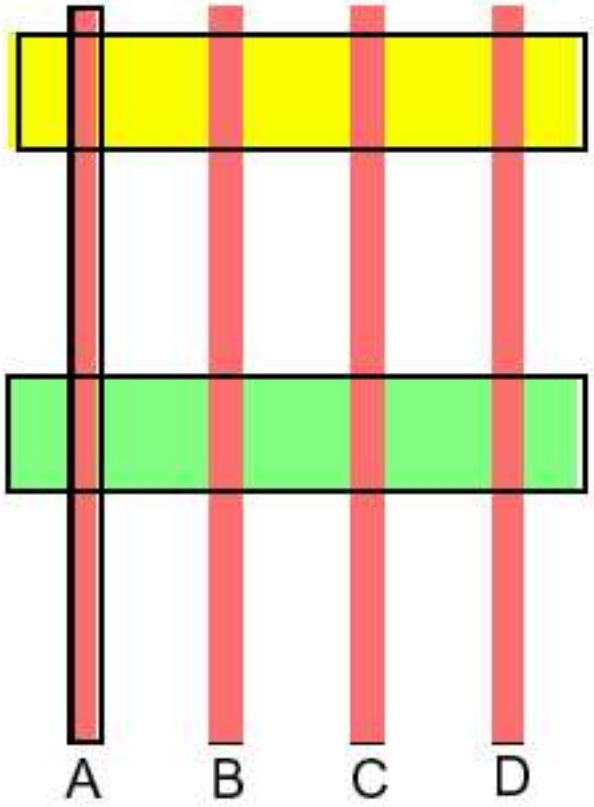
NOT ALL LAYOUTS ARE CREATED EQUAL

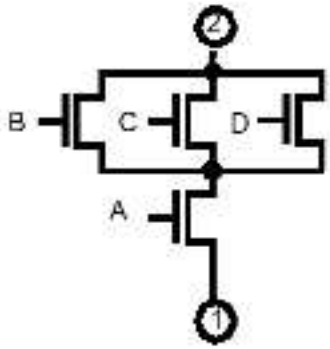


Let's look at two "equivalent" approaches

Examples: Layout <-> Circuit

NOT ALL LAYOUTS ARE CREATED EQUAL



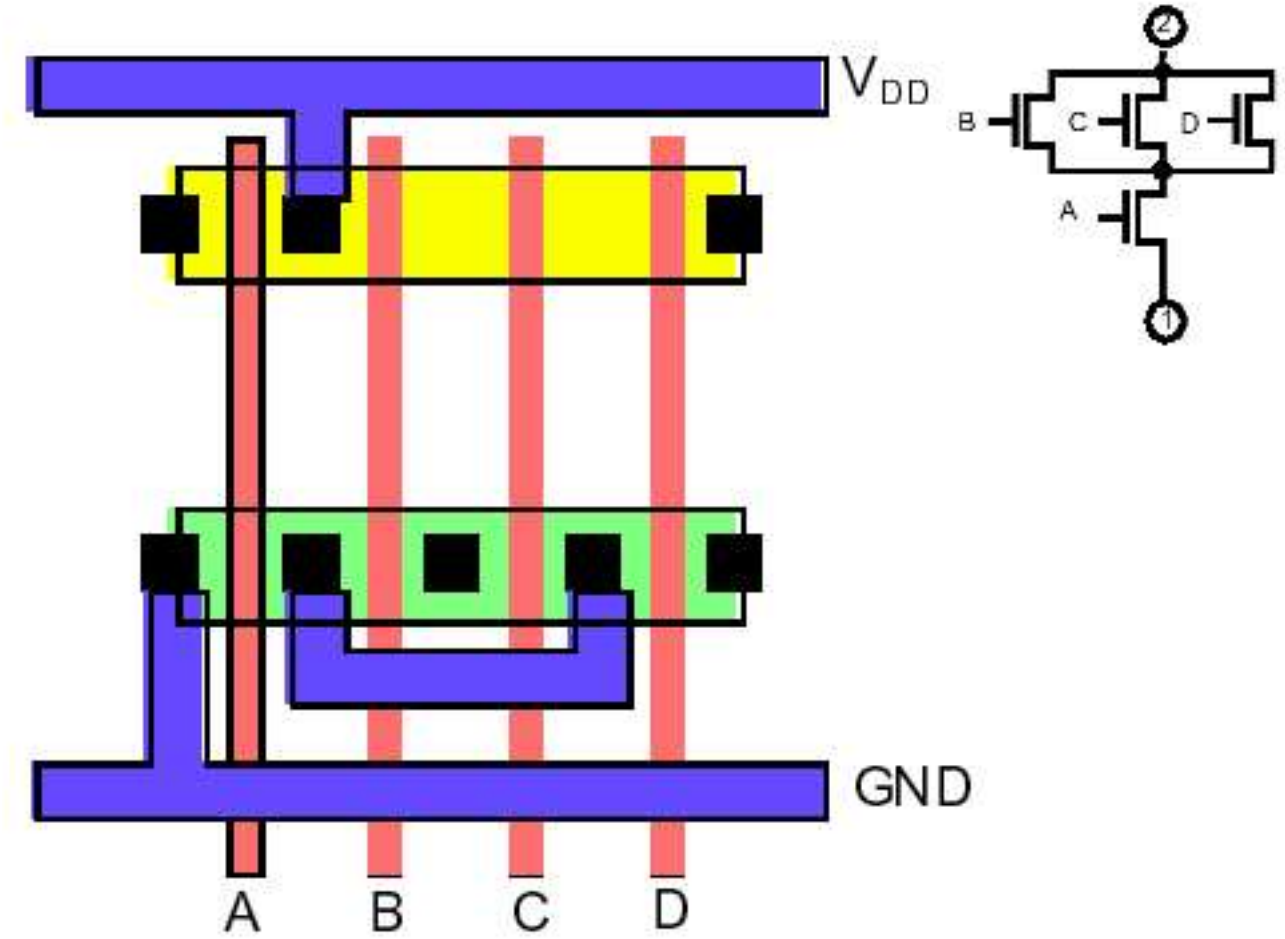


Bruce Jacob

University of
Maryland
ECE Dept.

Examples: Layout <-> Circuit

NOT ALL LAYOUTS ARE CREATED EQUAL

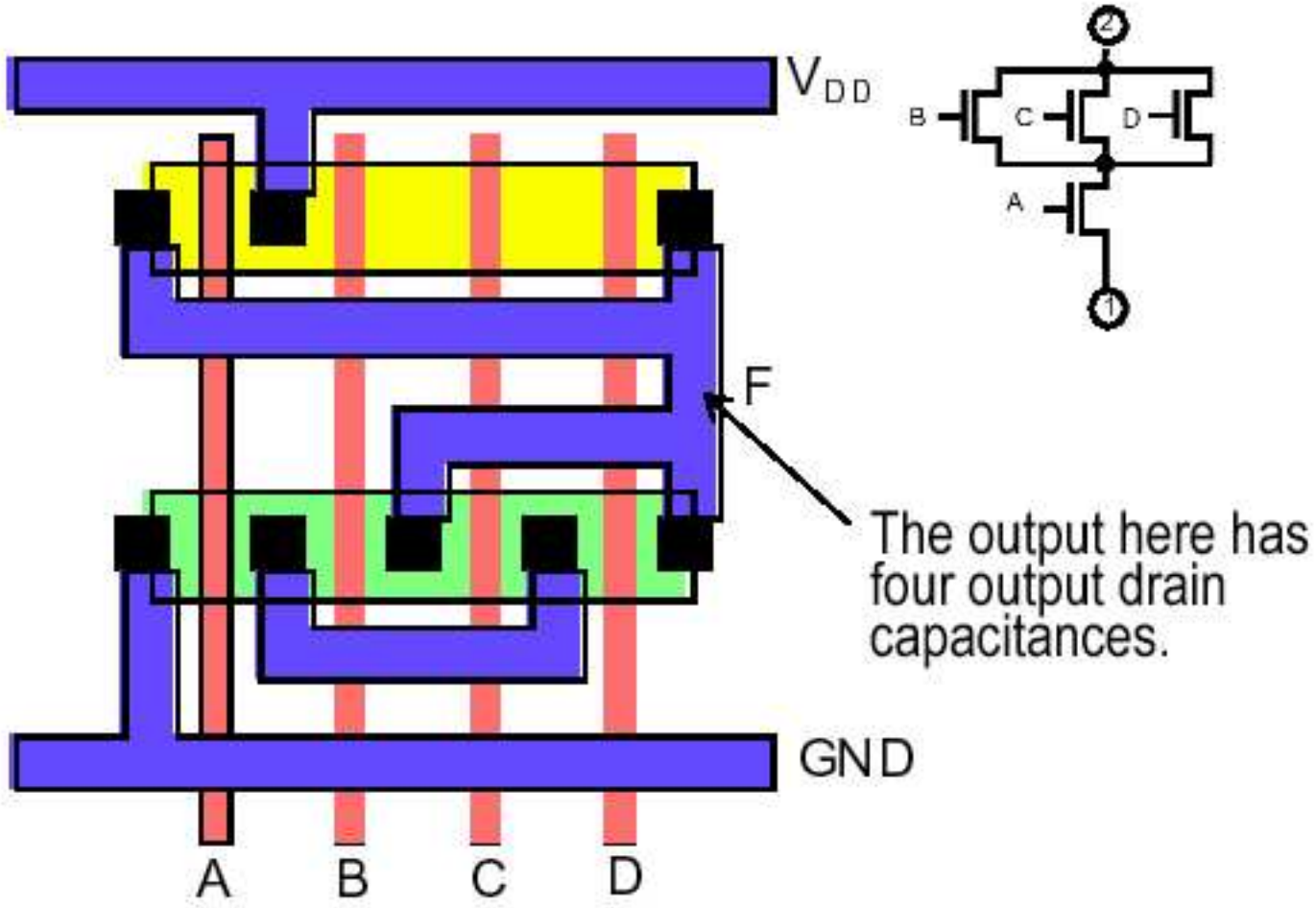


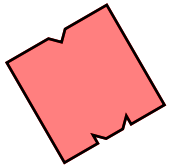
Bruce Jacob

University of
Maryland
ECE Dept.

Examples: Layout <-> Circuit

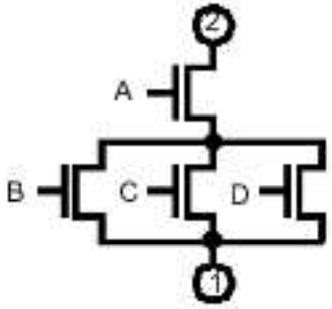
NOT ALL LAYOUTS ARE CREATED EQUAL



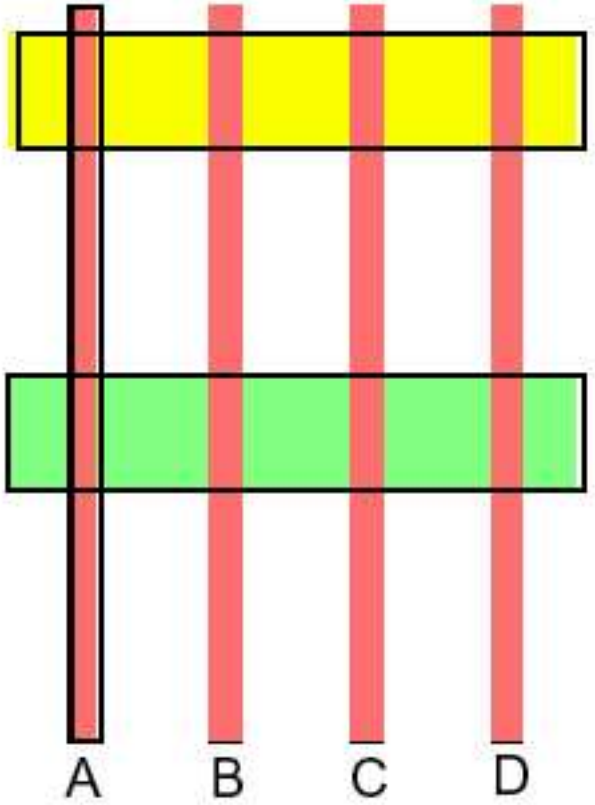


Examples: Layout <-> Circuit

NOT ALL LAYOUTS ARE CREATED EQUAL



Another design of same gate (circuit above simply flipped)

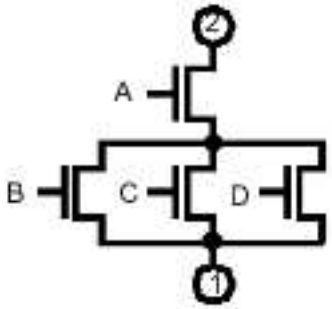


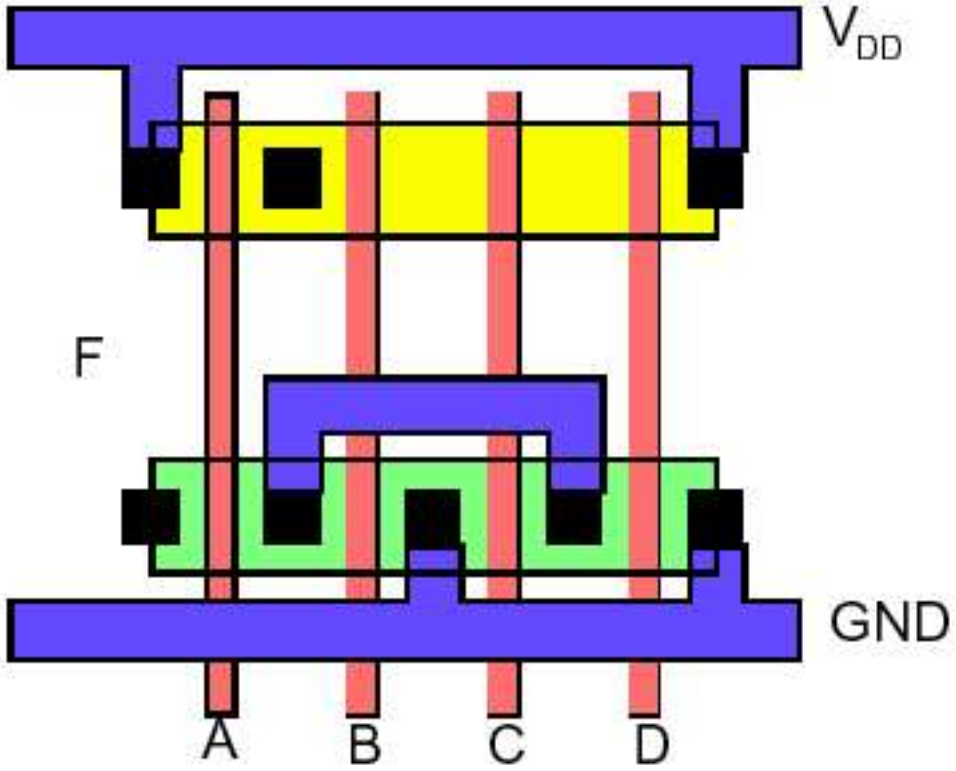
Bruce Jacob

University of
Maryland
ECE Dept.

Examples: Layout <-> Circuit

NOT ALL LAYOUTS ARE CREATED EQUAL



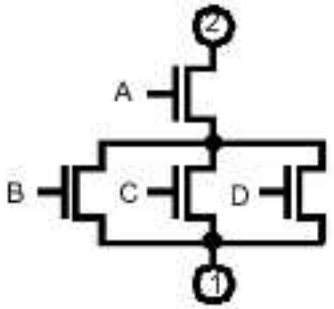


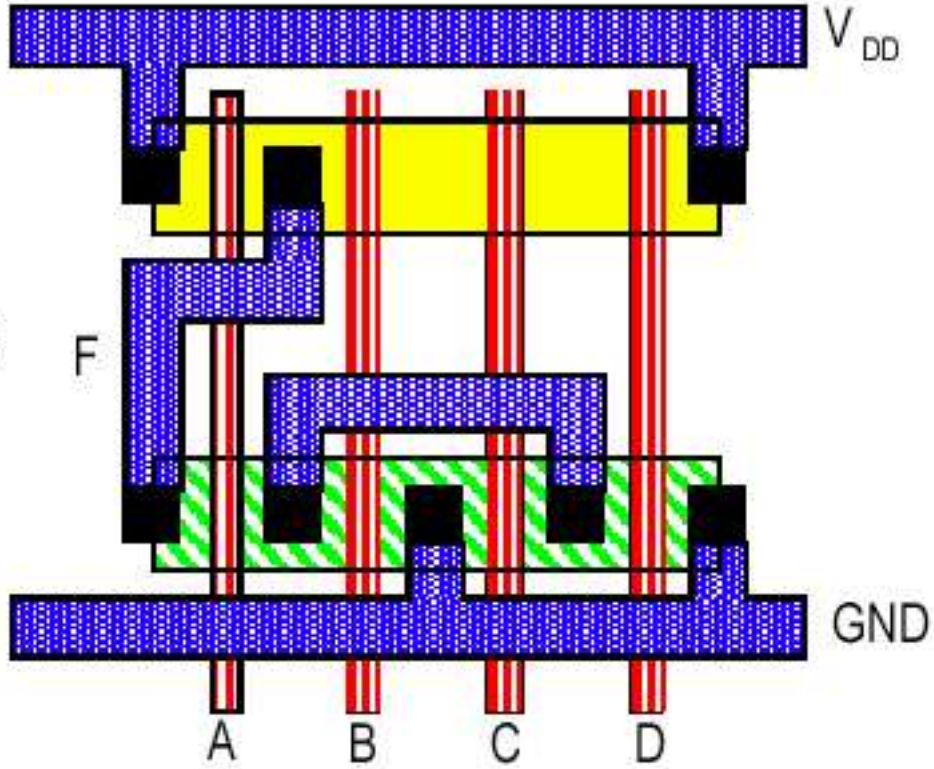
Bruce Jacob

University of
Maryland
ECE Dept.

Examples: Layout <-> Circuit

NOT ALL LAYOUTS ARE CREATED EQUAL





The output here has two output drain capacitances.

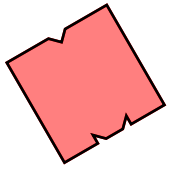
Bruce Jacob

University of Maryland
ECE Dept.

Examples: Layout <-> Circuit

Gate Design Procedure

- Run VDD & GND in metal at top & bottom
- Run vertical poly for each gate input
- Order gates to allow maximum source-drain abutting
- Place max # n-diffusions close to GND
- Place max # p-diffusions close to VDD
- Make remaining connections with metal (try to minimize metal usage)

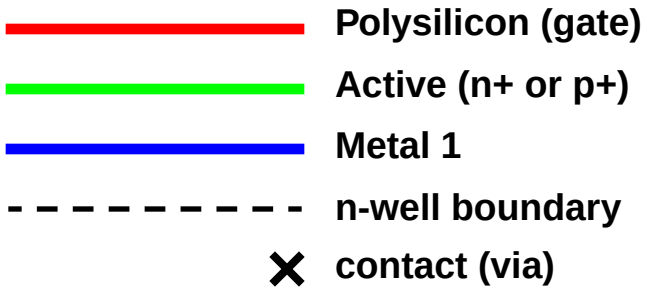


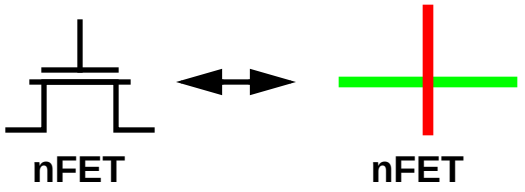
Bruce Jacob

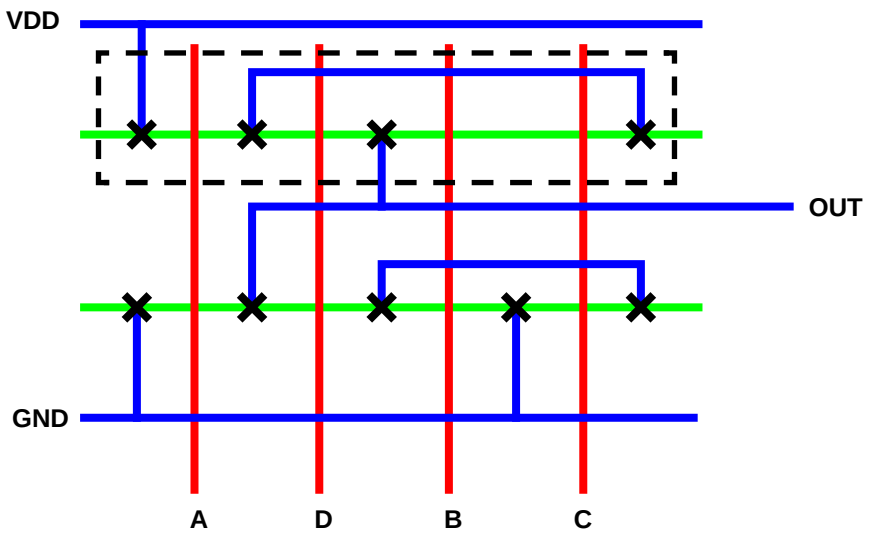
University of
Maryland
ECE Dept.

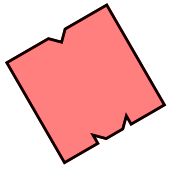
Stick Diagrams

- **Introduced by Mead & Conway in 80's**
- **Every line of conduction-material layer is represented by line of distinct color**





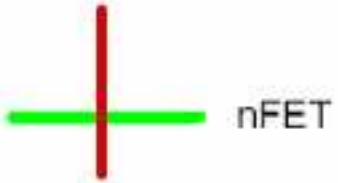




Stick Diagrams

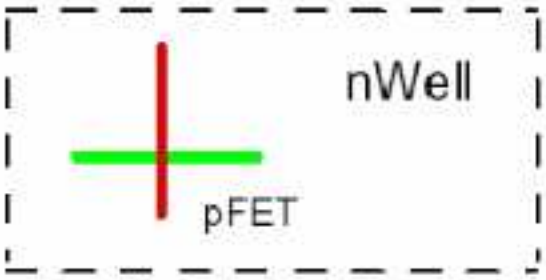
In terms of stick diagrams, we thus say that an nFET is formed whenever

Red (Poly) crosses over Green (Active)



This is consistent with a top view of the transistor.

A pFET is described by the same "red over green" coding, but the crossing point is contained within an nWell boundary



Bruce Jacob

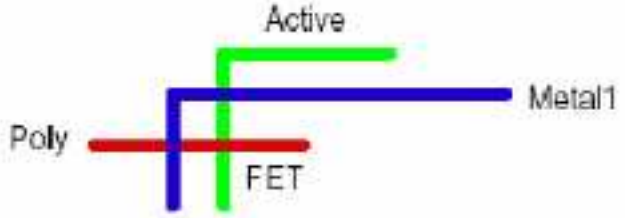
University of
Maryland
ECE Dept.

Stick Diagrams

The rules for constructing stick diagrams are based on the characteristics of the conducting layers.

- Only the routing is important, not the line widths
- Red over green gives a FET
  (Poly) (Active)

- Blue may cross over green or red without a connection
  (Metal1) (Active) (Poly)

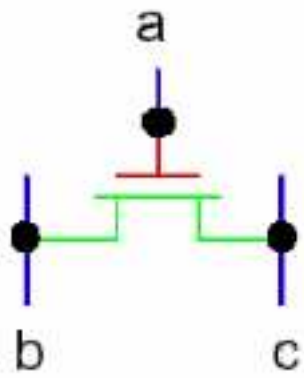


Bruce Jacob

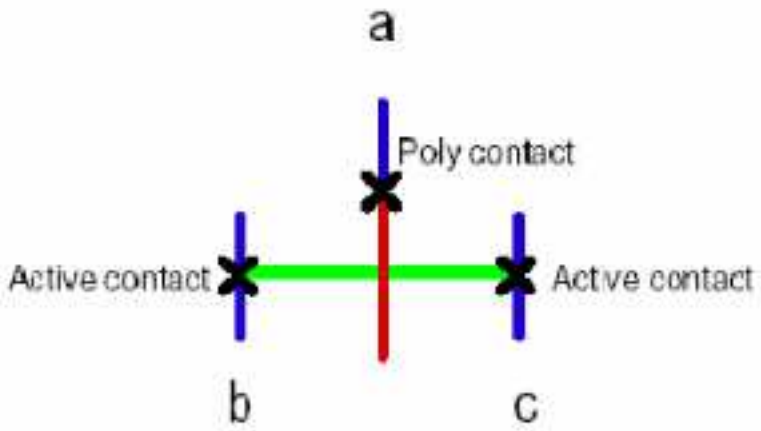
University of
Maryland
ECE Dept.

Stick Diagrams

Connections between layers are specified by ✖

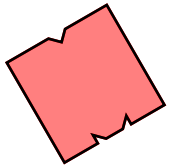


Schematic



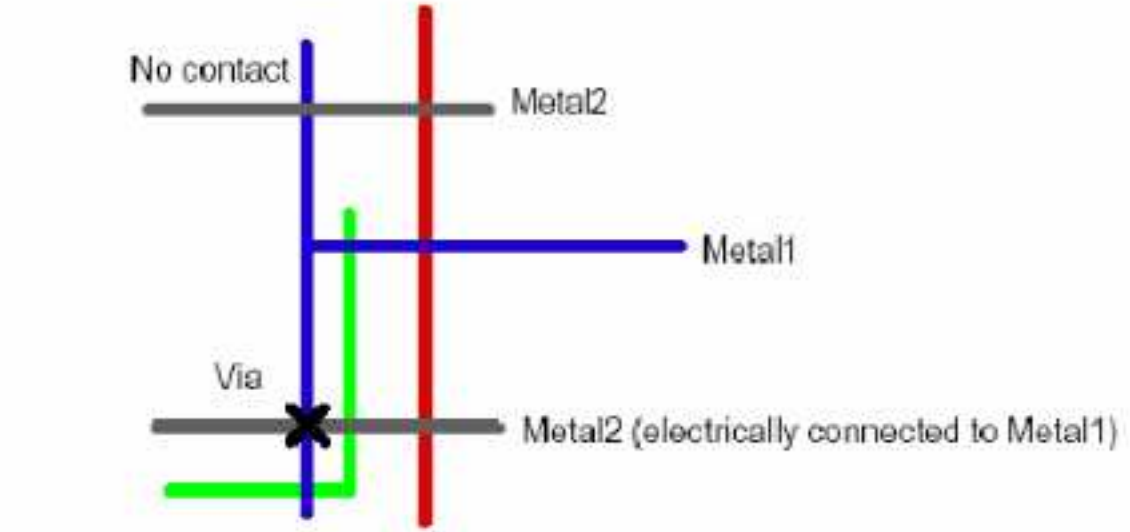
Stick diagram

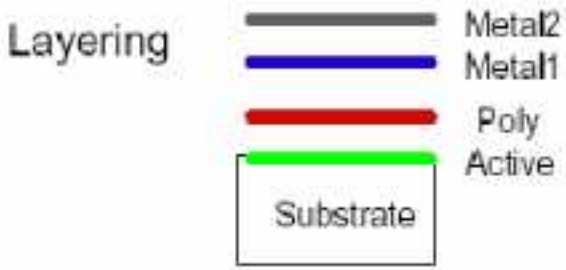
Poly contact: Metal1-to-Poly
Active Contact: Metal1-to-Active



Stick Diagrams

Metal lines on different layers can cross one another.
Contacting two metal lines requires a via



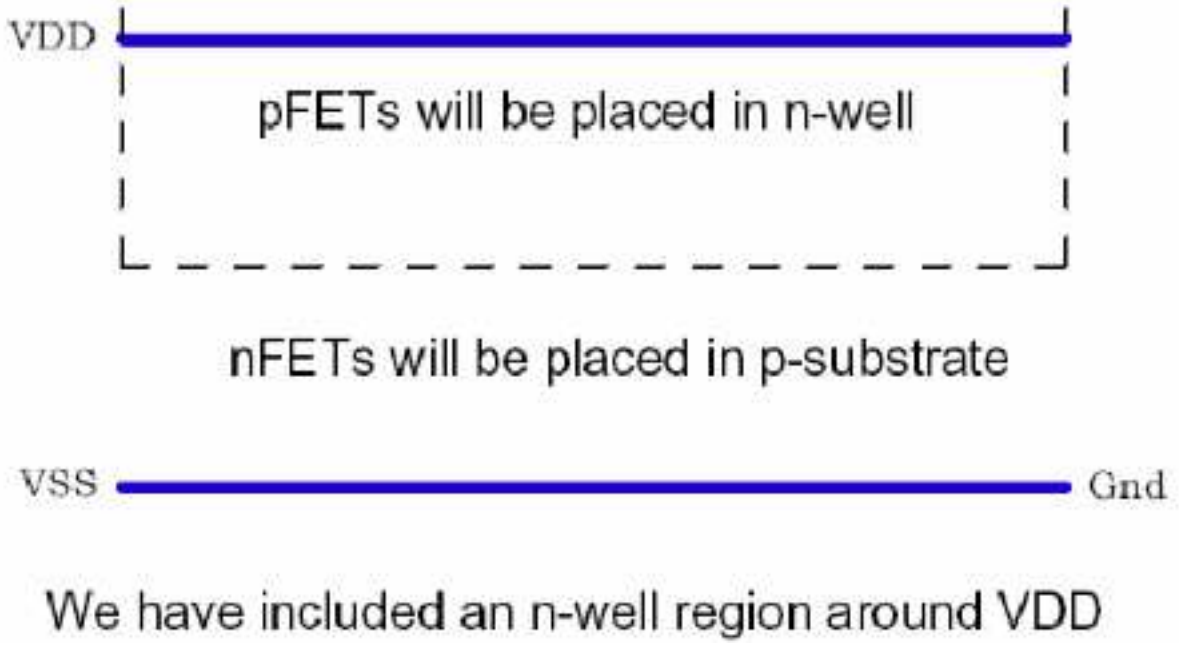


Bruce Jacob

University of Maryland
ECE Dept.

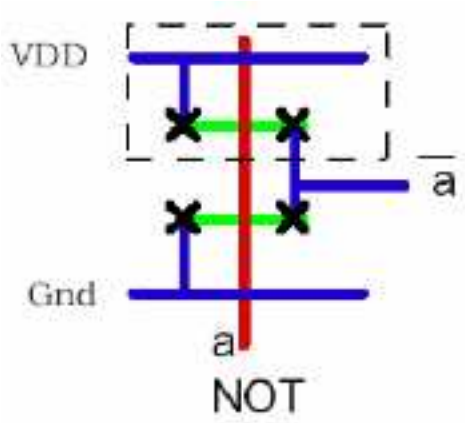
Stick Diagrams

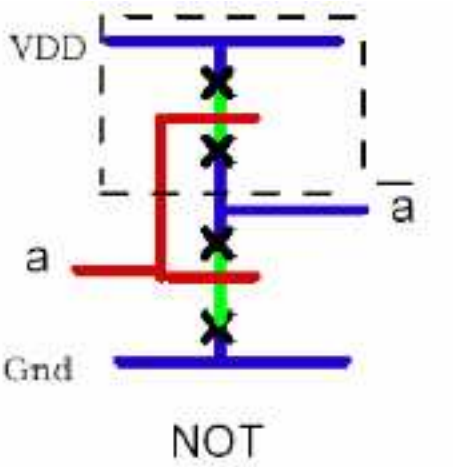
To create CMOS logic gates, we start with the VDD and VSS (ground) lines. We will use a horizontal orientation for the lines. Remember that stick diagrams only deal with the routing. Widths and spacings are not important.

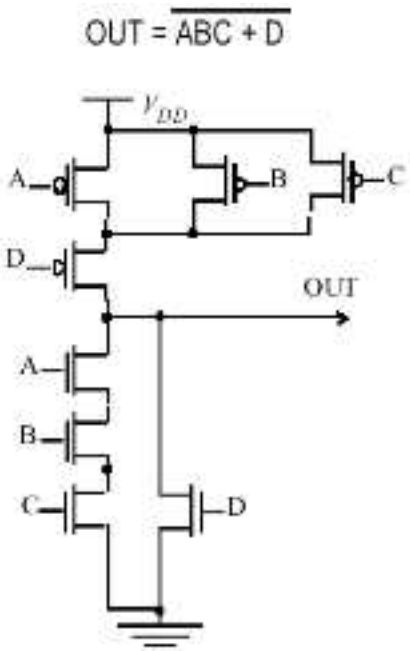


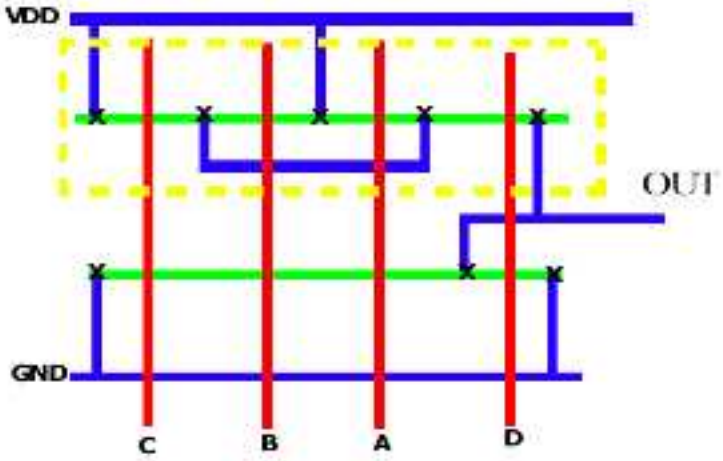
We have included an n-well region around VDD

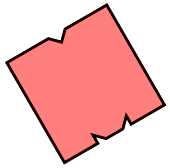
Stick Diagrams









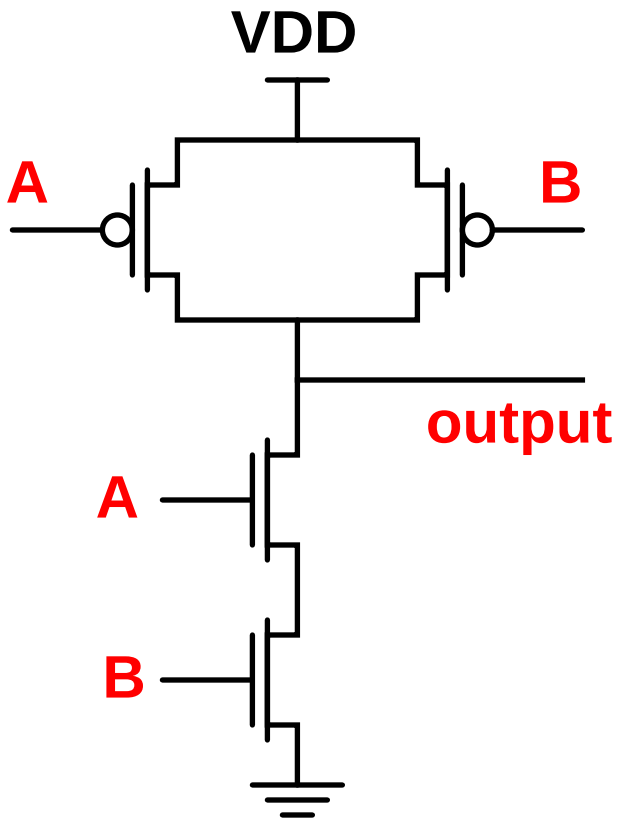


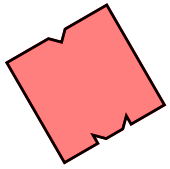
Bruce Jacob

University of
Maryland
ECE Dept.

Examples

2-input NAND



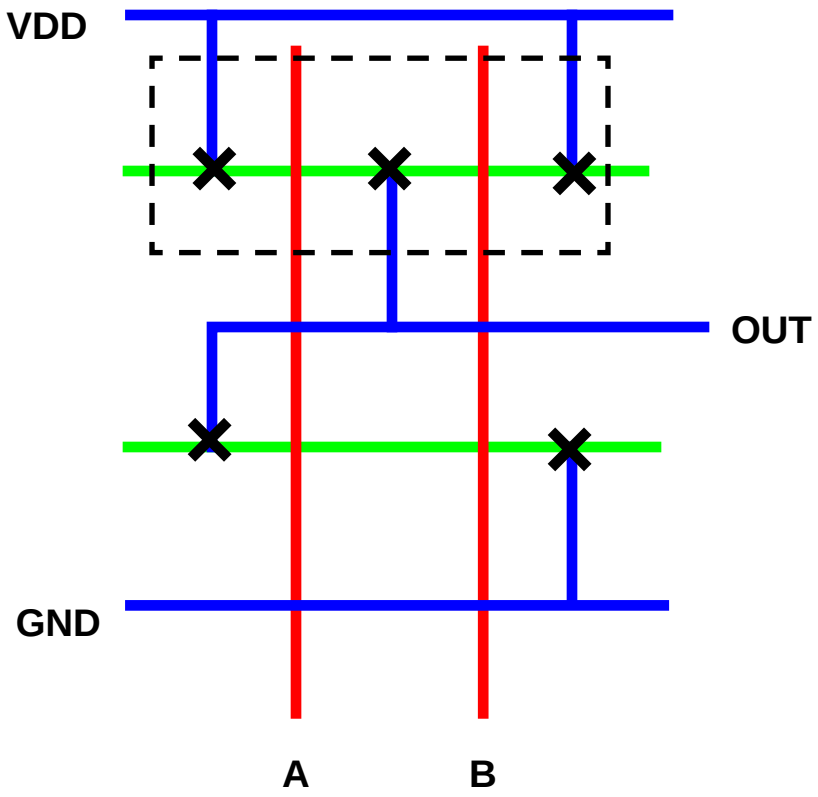


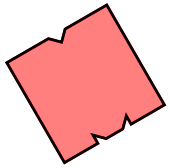
Bruce Jacob

University of
Maryland
ECE Dept.

Examples

2-input NAND



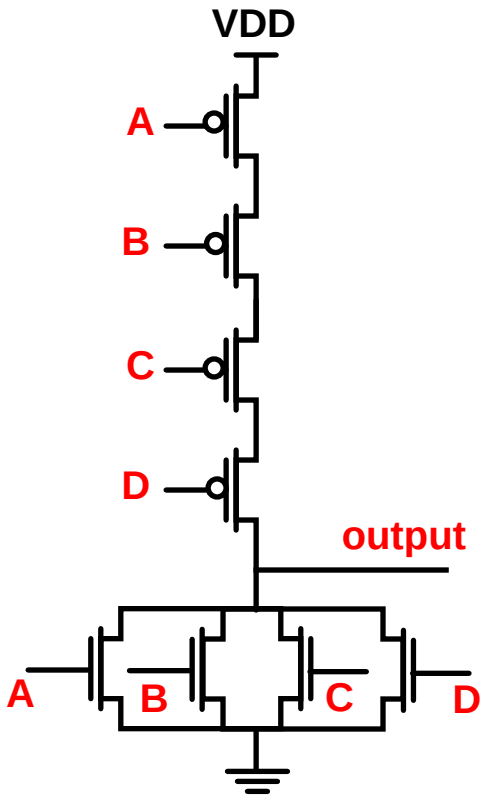


Bruce Jacob

University of
Maryland
ECE Dept.

Examples

4-input NOR

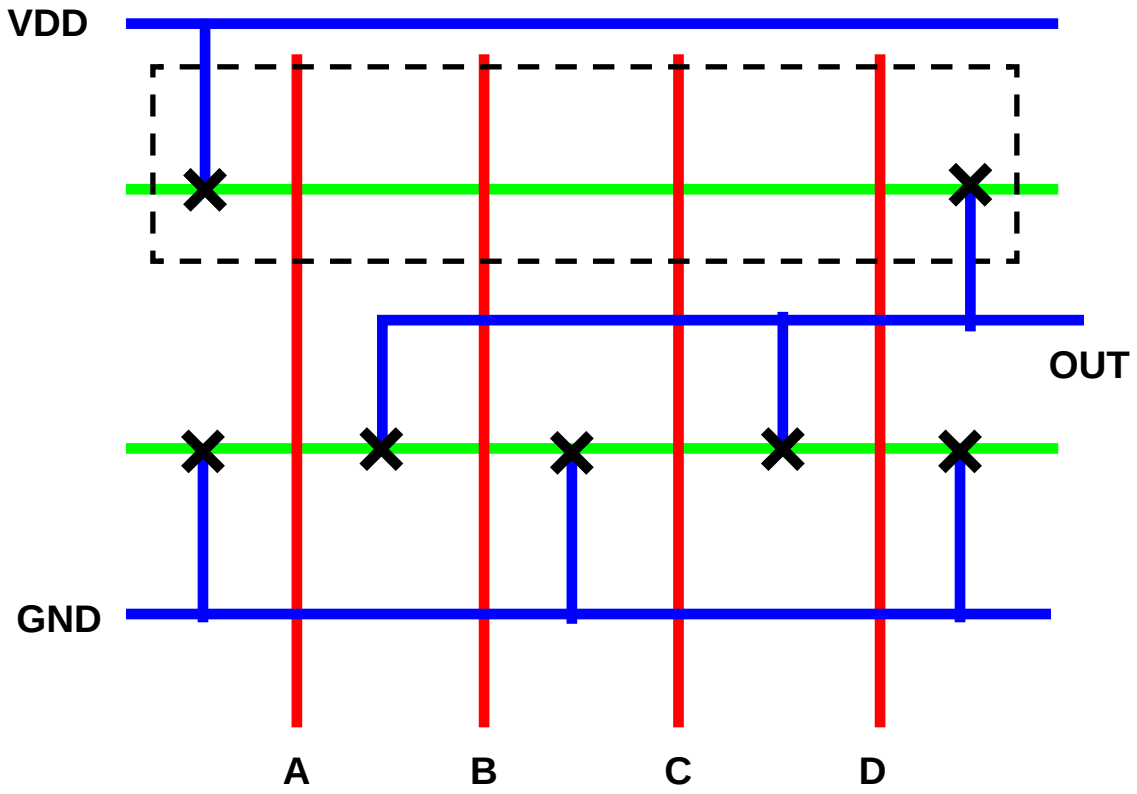


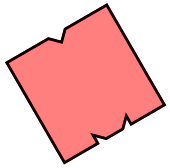
Bruce Jacob

University of
Maryland
ECE Dept.

Examples

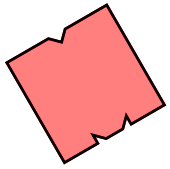
4-input NOR





Examples

out = ~(A • (C + BD))

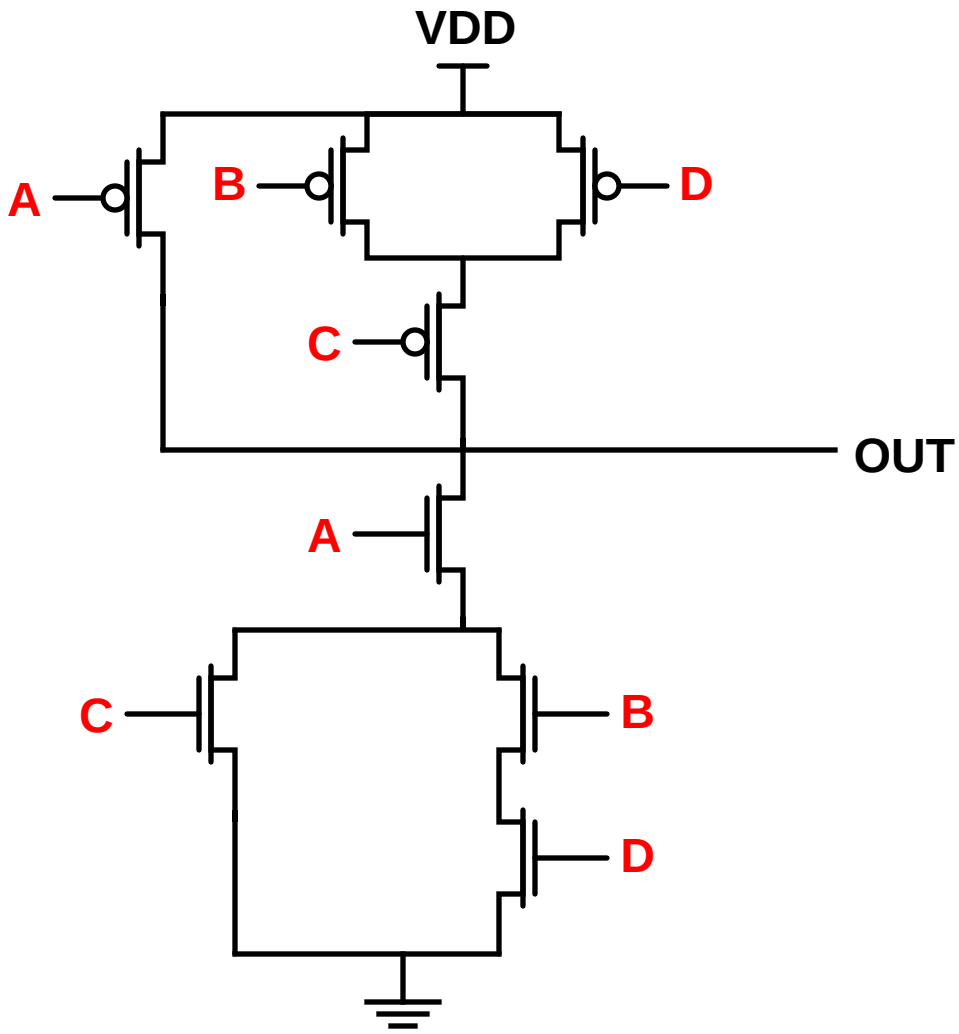


Bruce Jacob

University of
Maryland
ECE Dept.

Examples

out = ~(A • (C + BD))

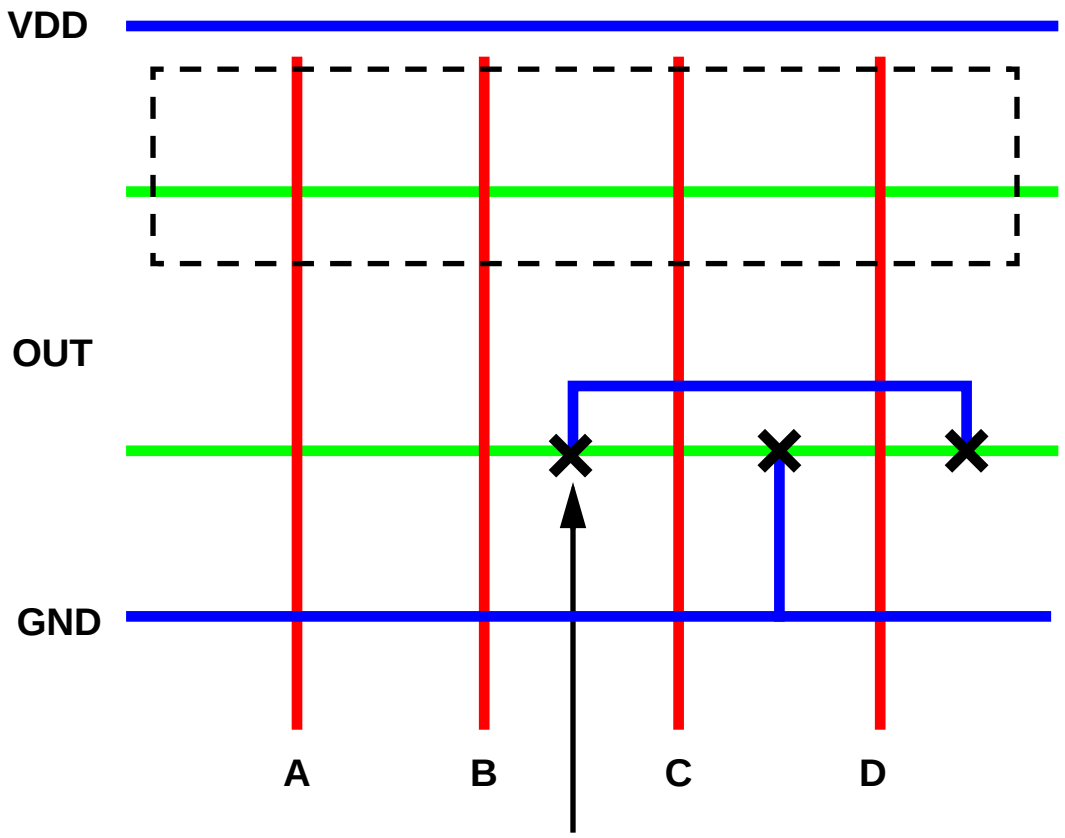


Bruce Jacob

University of
Maryland
ECE Dept.

Examples

out = ~(A • (C + BD))



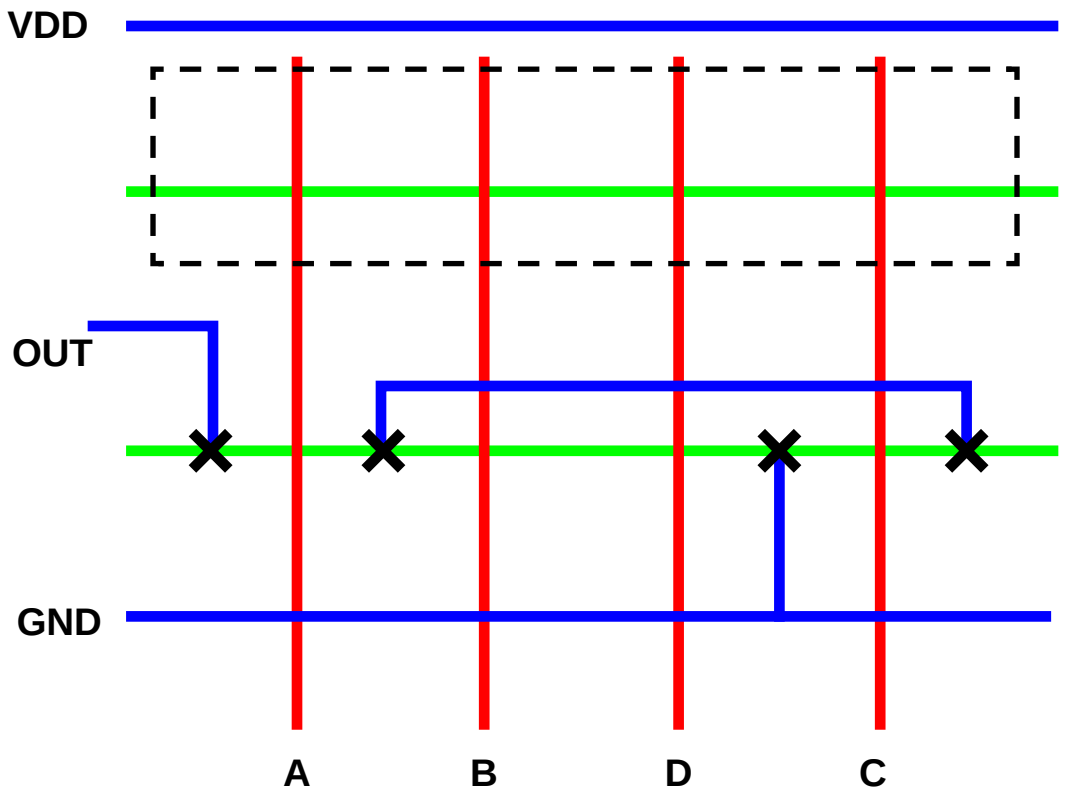
OOOPS -- can't do this

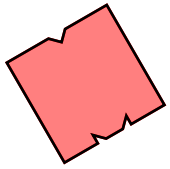
Bruce Jacob

University of
Maryland
ECE Dept.

Examples

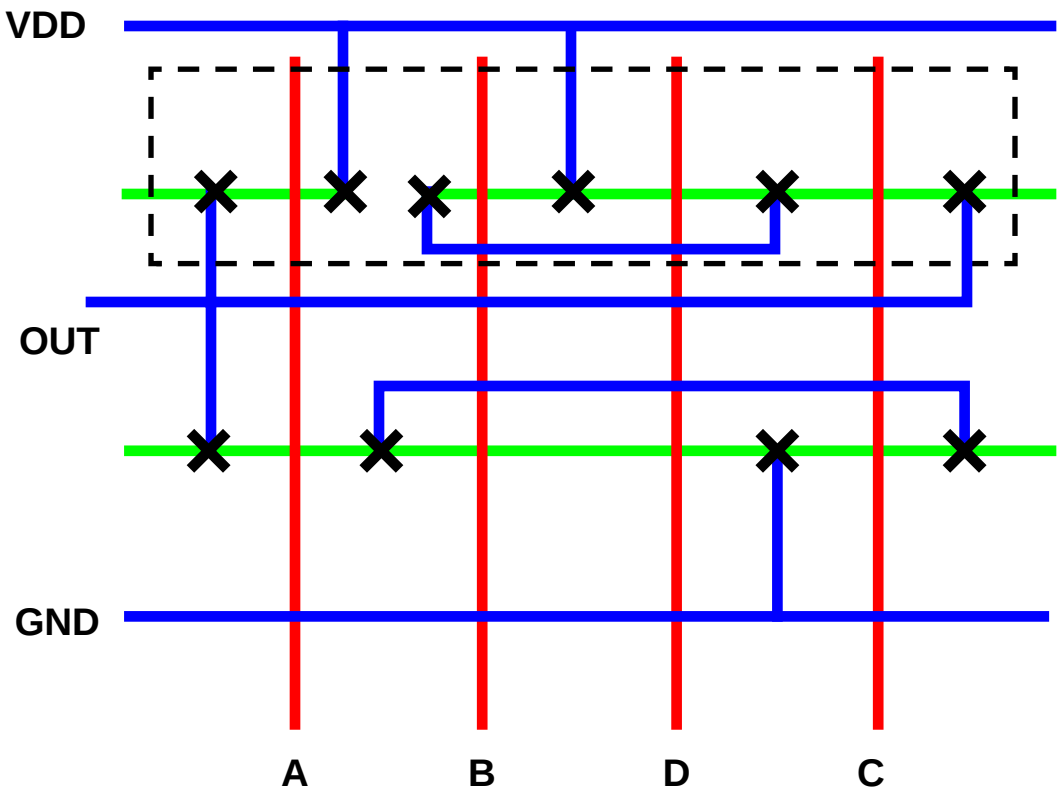
out = ~(A • (C + BD))



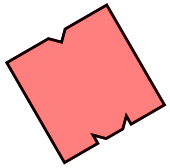


Examples

out = ~(A • (C + BD))



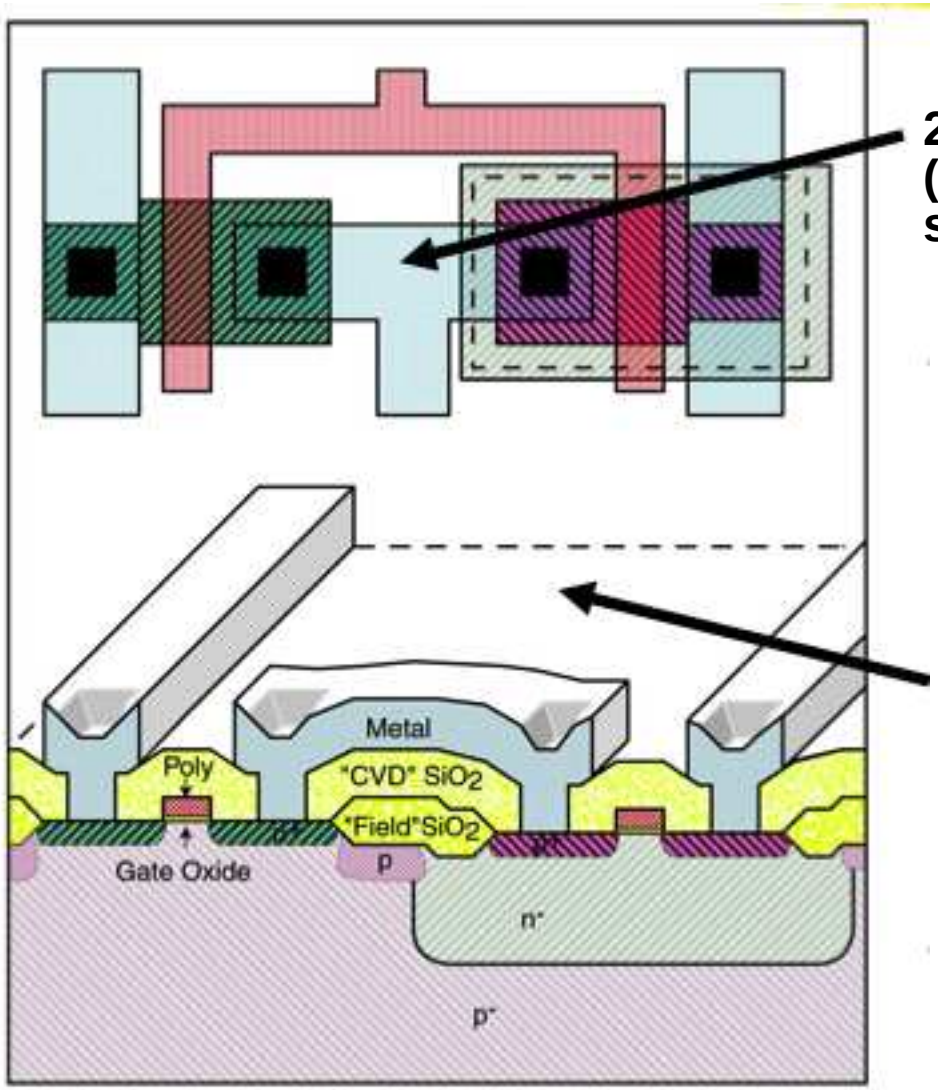
For PUN, either re-route poly or cut p-diff



Bruce Jacob

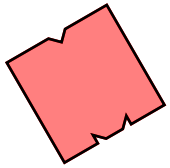
University of
Maryland
ECE Dept.

Views of a Design



2D top-down view (how designers see the chip)

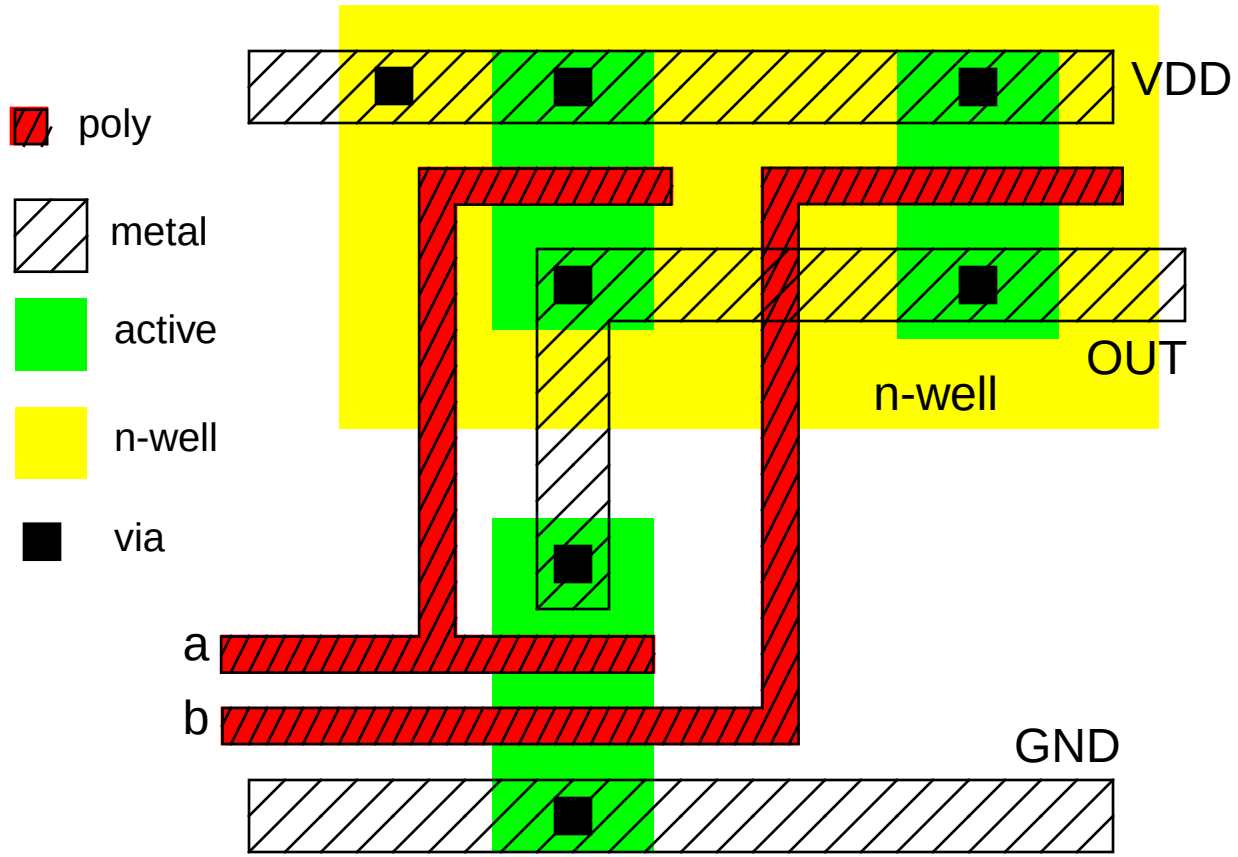
3D cross section (how process engineers see the chip)



Bruce Jacob

University of
Maryland
ECE Dept.

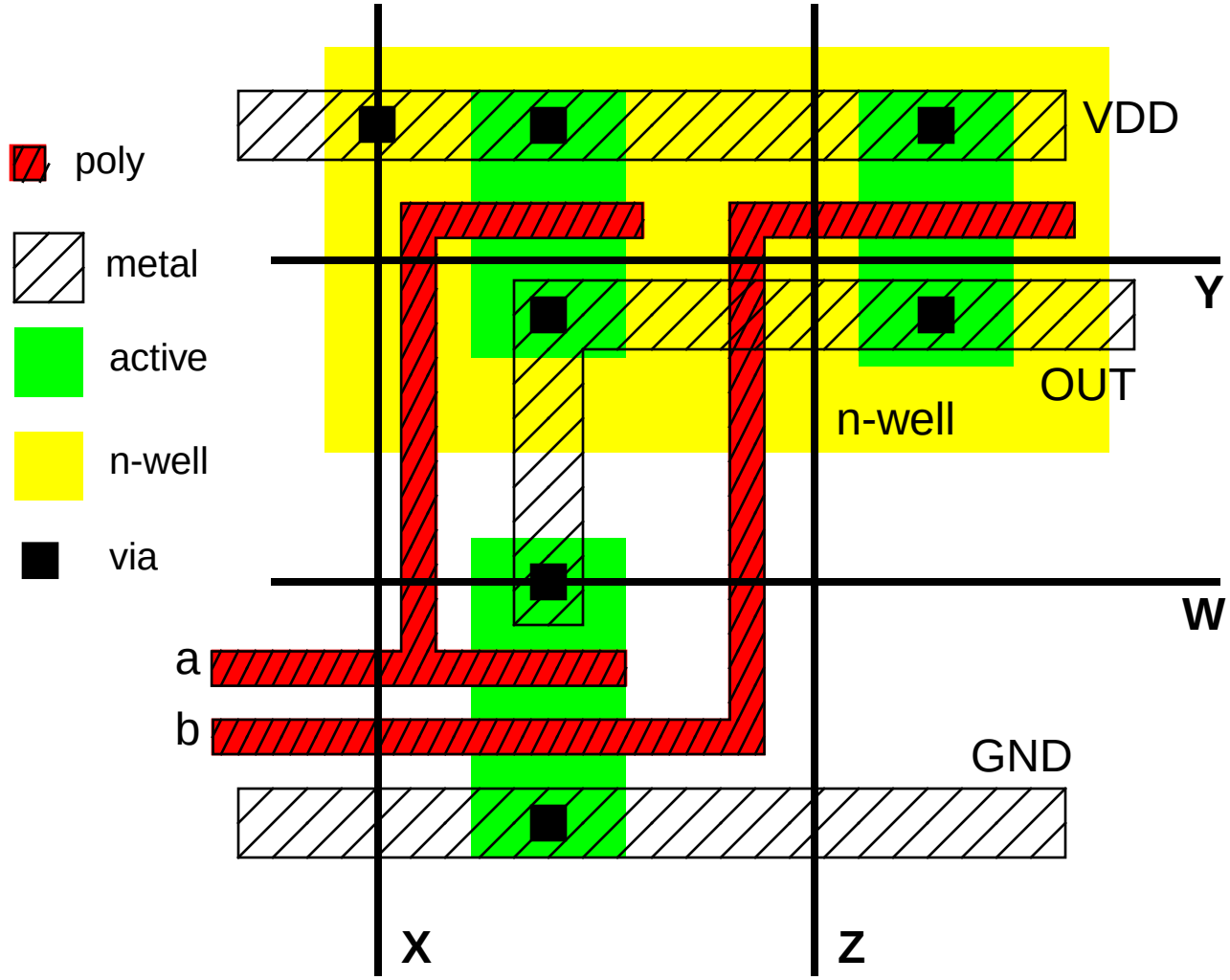
Examples



Bruce Jacob

University of
Maryland
ECE Dept.

Examples



Sizing: What is a MOSFET?

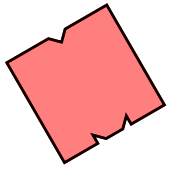
A resistor: $$R_n = \frac{1}{\mu_n C_{ox}(V_{GS} - V_{Tn})}\left(\frac{L}{W}\right)$$

- **(among other things ...) Increasing W decreases the resistance; allows more current to flow**

Oxide capacitance $C_{ox} = \varepsilon_{ox} / t_{ox}$ **[F/cm^2]**

Transconductance $\beta_n = \mu_n C_{ox}\left(\frac{W}{L}\right) = k'_n\left(\frac{W}{L}\right)$

Gate capacitance $C_G = C_{ox} WL$ **[F]**



Bruce Jacob

University of
Maryland
ECE Dept.

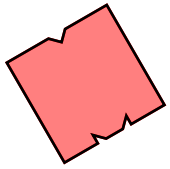
nFET vs. pFET

$$R_n = \frac{1}{\beta_n (V_{DD} - V_{Tn})} \qquad \beta_n = \mu_n C_{ox} \left(\frac{W}{L}\right)_n$$

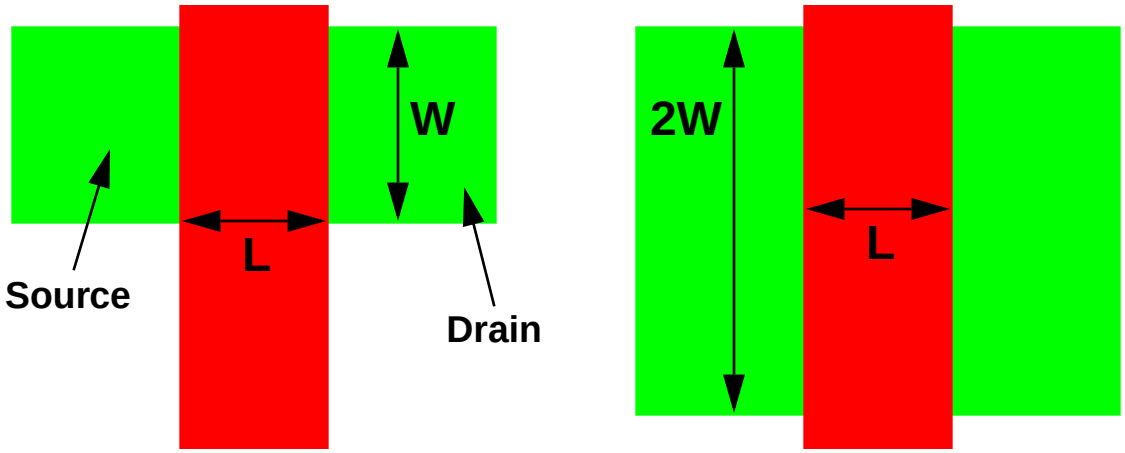
$$R_p = \frac{1}{\beta_p (V_{DD} - |V_{Tp}|)} \qquad \beta_p = \mu_p C_{ox} \left(\frac{W}{L}\right)_p$$

$$\frac{\mu_n}{\mu_p} = r$$ **Typically (2 .. 3)**

(μ is the carrier mobility through device)



Transistor Sizing I



The electrical characteristics of transistors determine the switching speed of a circuit

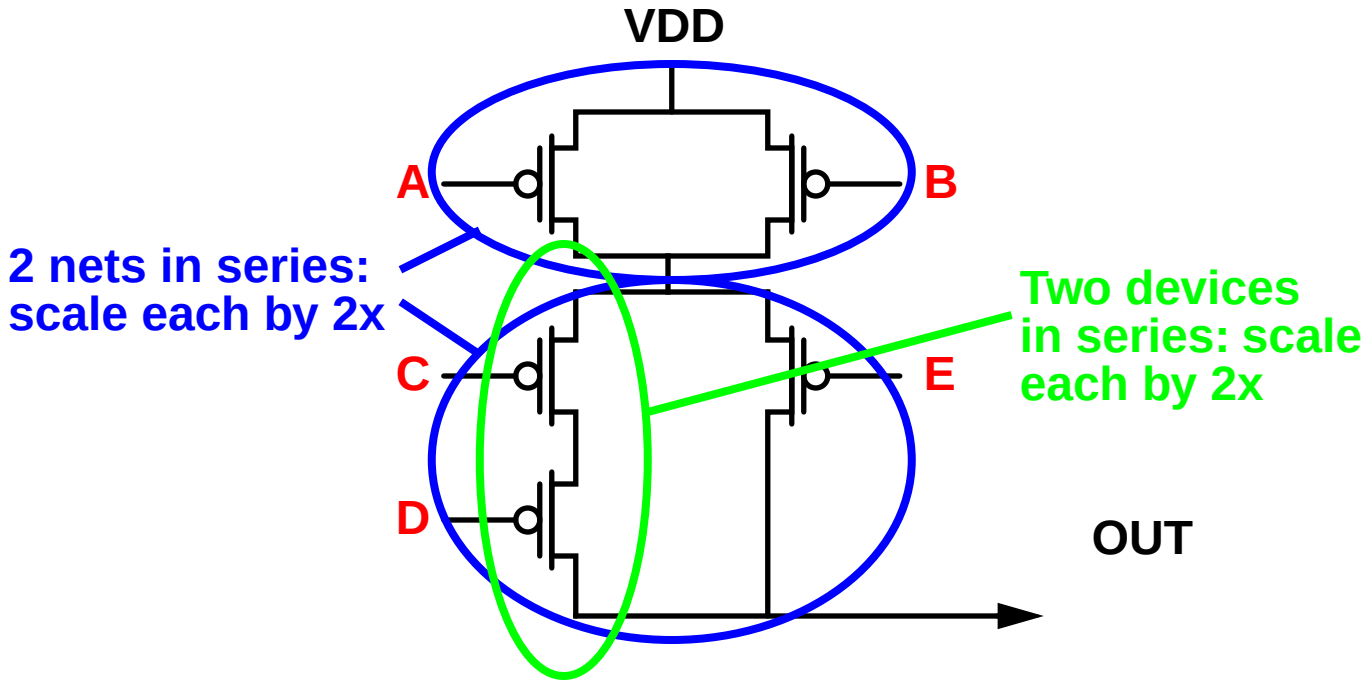
- **Need to select the aspect ratios $(W/L)_n$ and $(W/L)_p$ of *every* FET in the circuit**

Define *Unit Transistor* (R_1, C_1)

- **L/W_{min}-> highest resistance (needs scaling)**
- **$R_2 = R_1 \div 2$ and $C_2 = 2 \bullet C_1$**
- **Separate nFET and pFET unit transistors**
- **Unit devices are *not* restricted to individual transistors**

Sizing I: Complex Gates

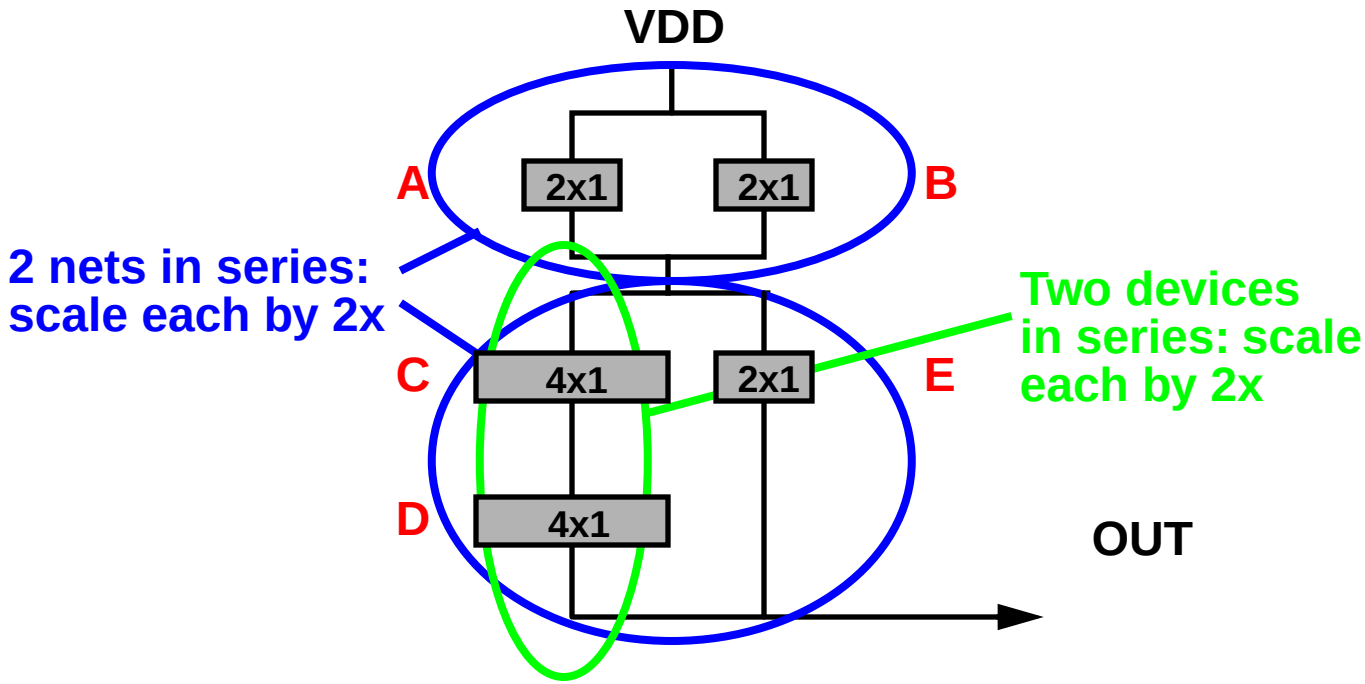
Critical transistors: those in series



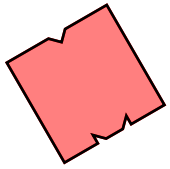
- N FETs in series => scale each by factor of N
- Ignore FETs in parallel (assume worst case: only 1 on)
- Ultimate goal: total resistance of net = 1 square

Sizing I: Complex Gates

Critical transistors: those in series



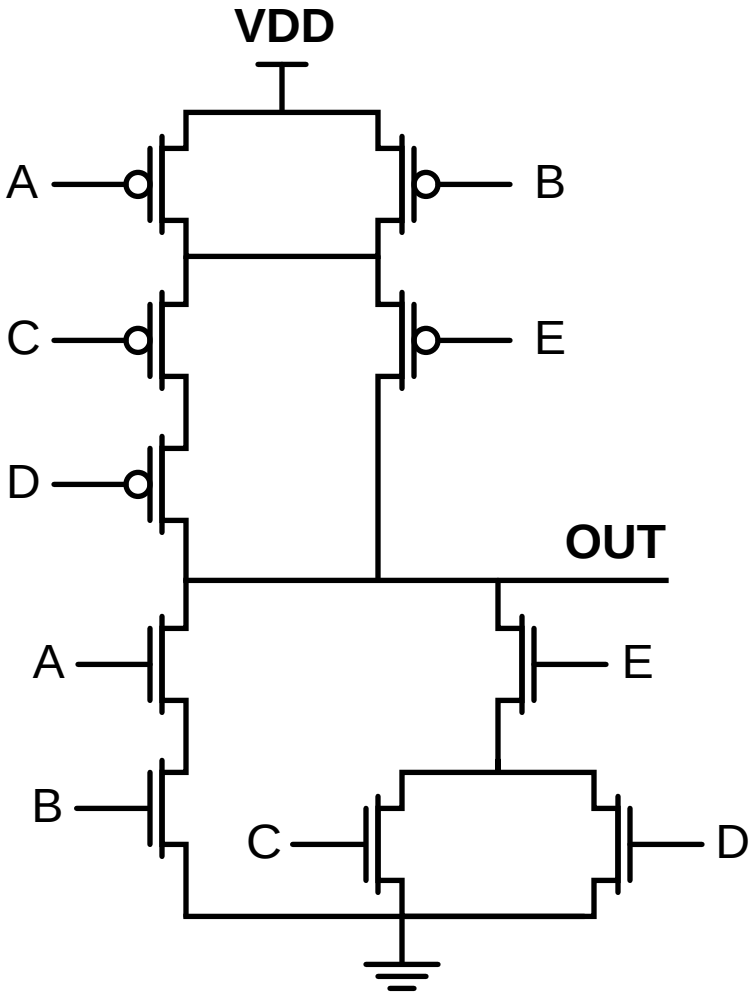
- N FETs in series => scale each by factor of N
- Ignore FETs in parallel (assume worst case: only 1 on)
- Ultimate goal: total resistance of net = 1 square

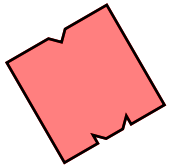


Bruce Jacob

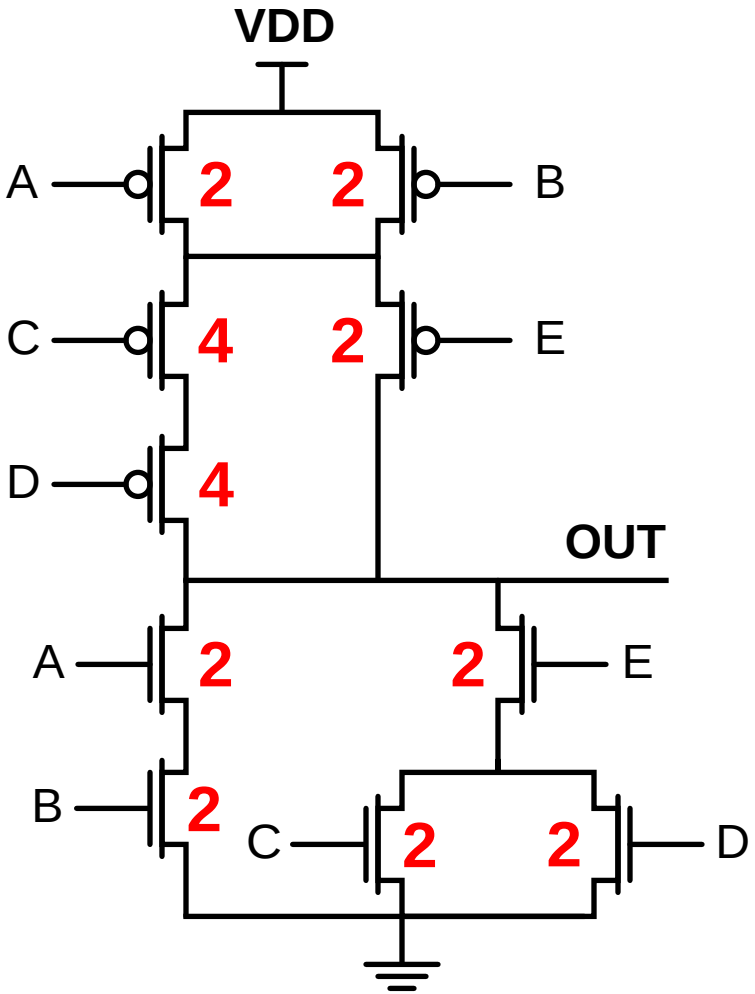
University of
Maryland
ECE Dept.

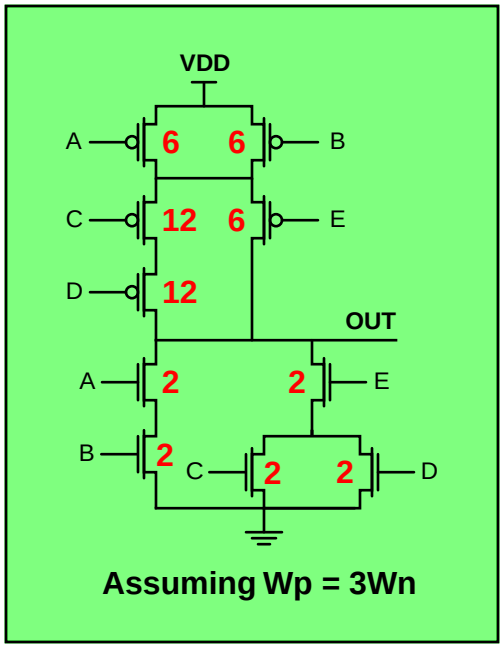
Examples





Examples

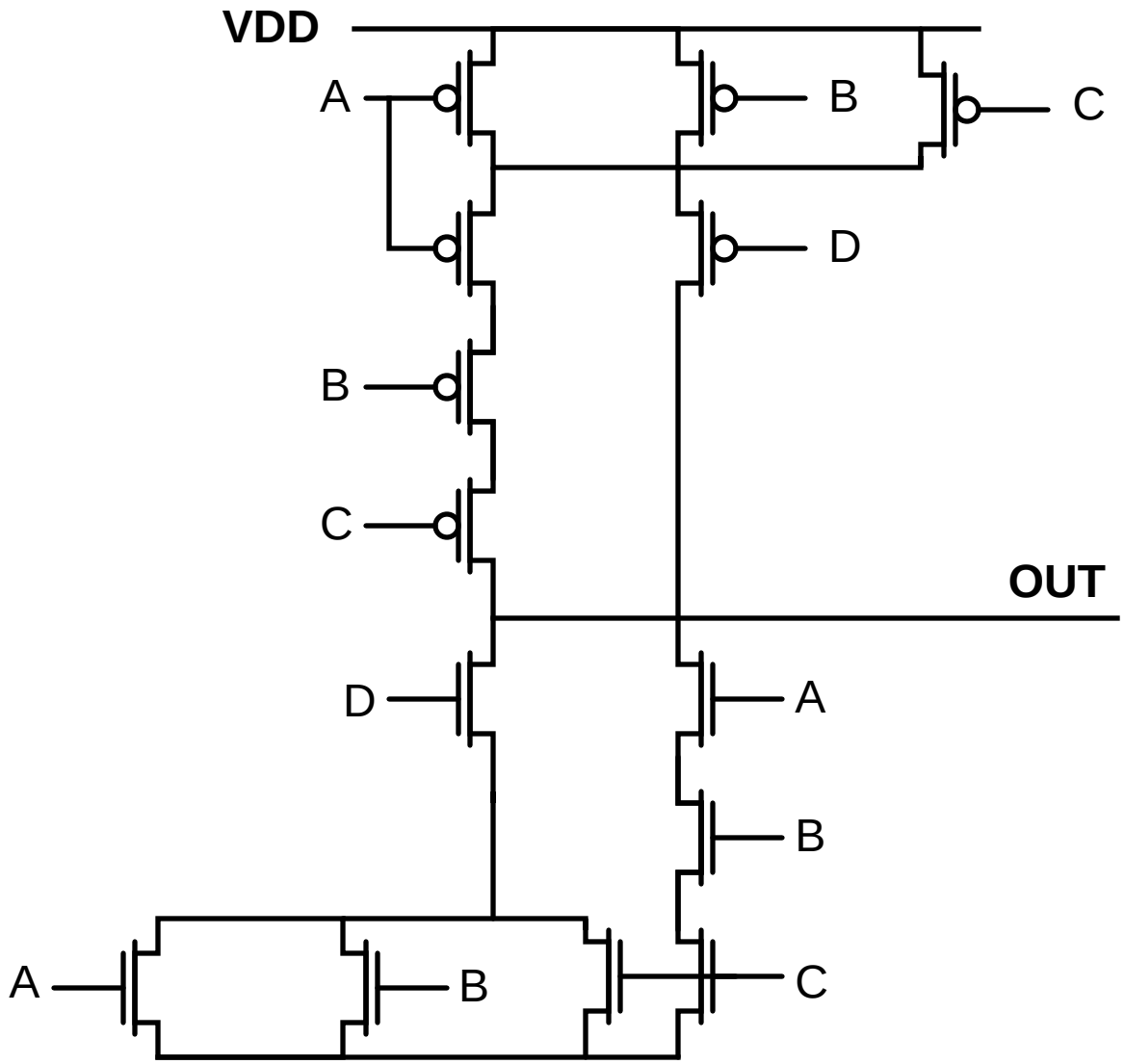

VDD
A
2
2
B
C
4
2
E
D
4
OUT
A
2
2
E
B
2
C
2
2
D


VDD
A
6
6
B
C
12
6
E
D
12
OUT
A
2
2
E
B
2
C
2
2
D
Assuming Wp = 3Wn

Bruce Jacob

University of
Maryland
ECE Dept.

Examples



Bruce Jacob

University of
Maryland
ECE Dept.

Examples