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ENEE 359a
Digital VLSI Design

CMOS Memories and Systems: Part II, DRAM Circuits

Prof. Bruce Jacob

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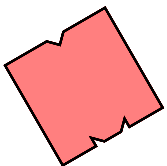
Credit where credit is due:
Slides contain original artwork (© Jacob 1999–2004, Wang 2003/4) as well as material taken from Keeth & Baker's DRAM Circuit Design.



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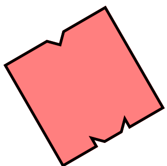
Overview

DRAM:

- DRAM systems
- DRAM circuits

SRAM:

- SRAM systems
- SRAM circuits
- Register files



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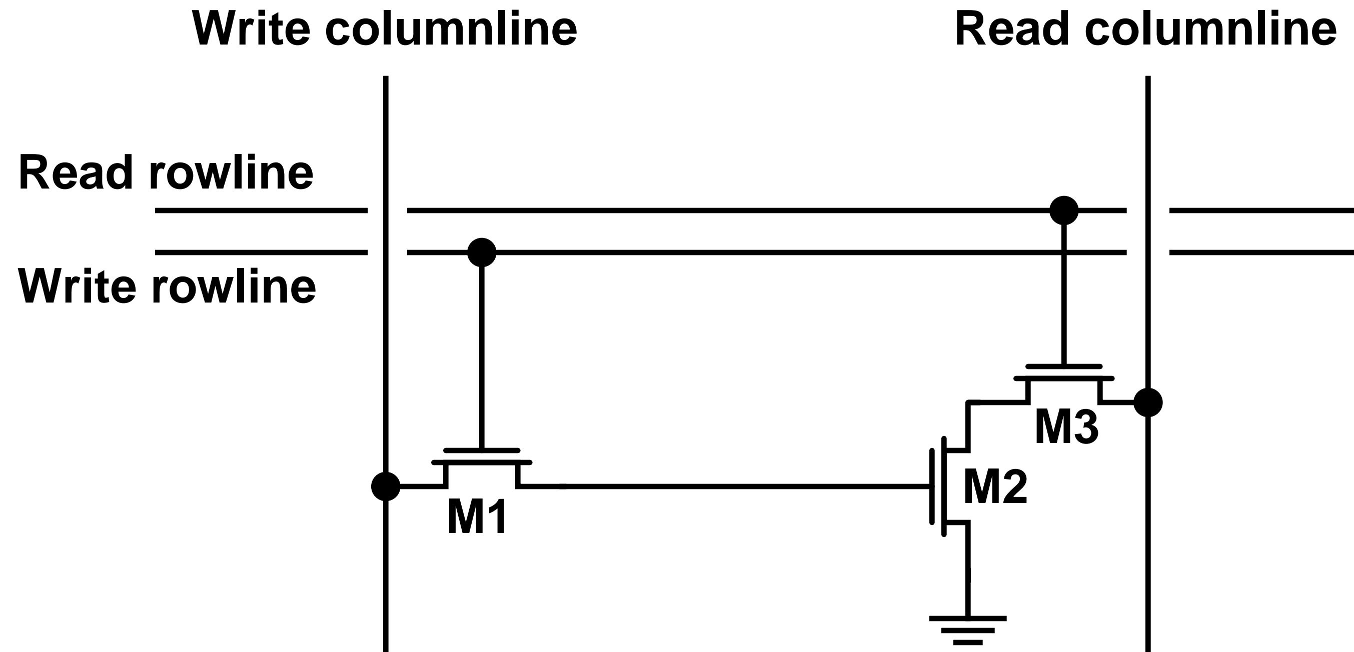
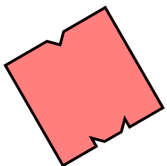
The Original 3T DRAM Cell



First generation DRAM cell

- MOSFET #2 is used as storage node (obvious to see why “dynamic”)
- Read columnline precharged for read; line either pulled to GND or not.



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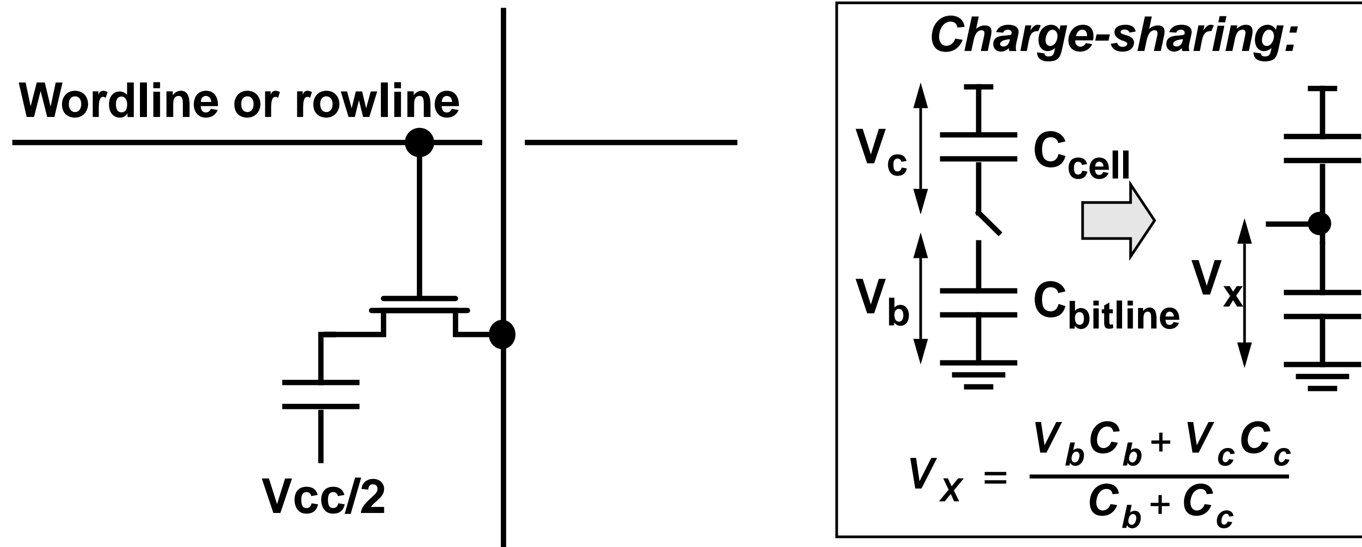
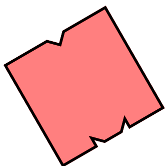
Second Generation 1T1C Cell



- **Wordline can be polysilicon; MOSFET formed by wordline over n+ active area**
- **To write full Vcc to storage capacitor, rowline (gate) must be driven to voltage Vccp > Vcc + Vth**
- **Bitline can be metal or polysilicon**
- **Charge-sharing: what potential should be at other side of storage capacitor? (e.g. $V_0 = 0$, $V_1 = Vcc$)**



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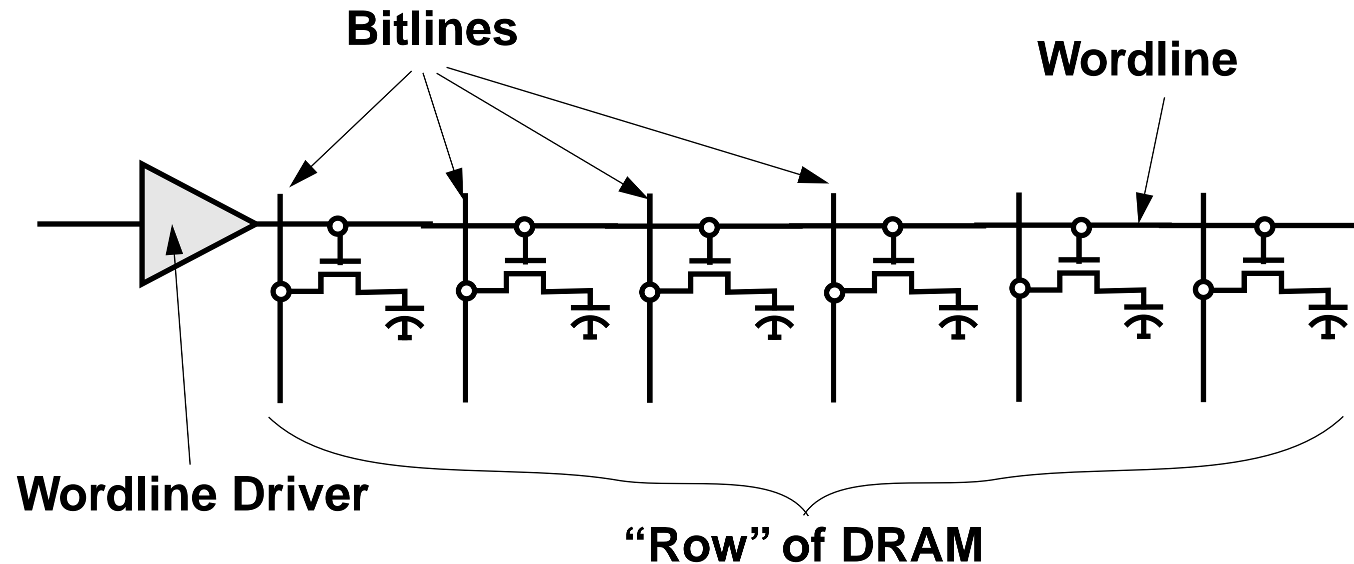
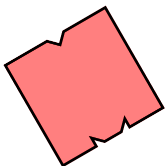
Wordline



Wordline presents large capacitive load; slow, limits t_{RC} (time to open & close row)

- **Use wordline driver: large FETs (remember scaling?)**
- **Polysilicon wordline usually topped with silicide ("polycide" wordline); increases conductivity**
- **Additional drivers can be placed along length**
- **Wordline can be "stitched" with pieces of metal**
- **Typical organization: 512 wordlines x 512 bitlines**



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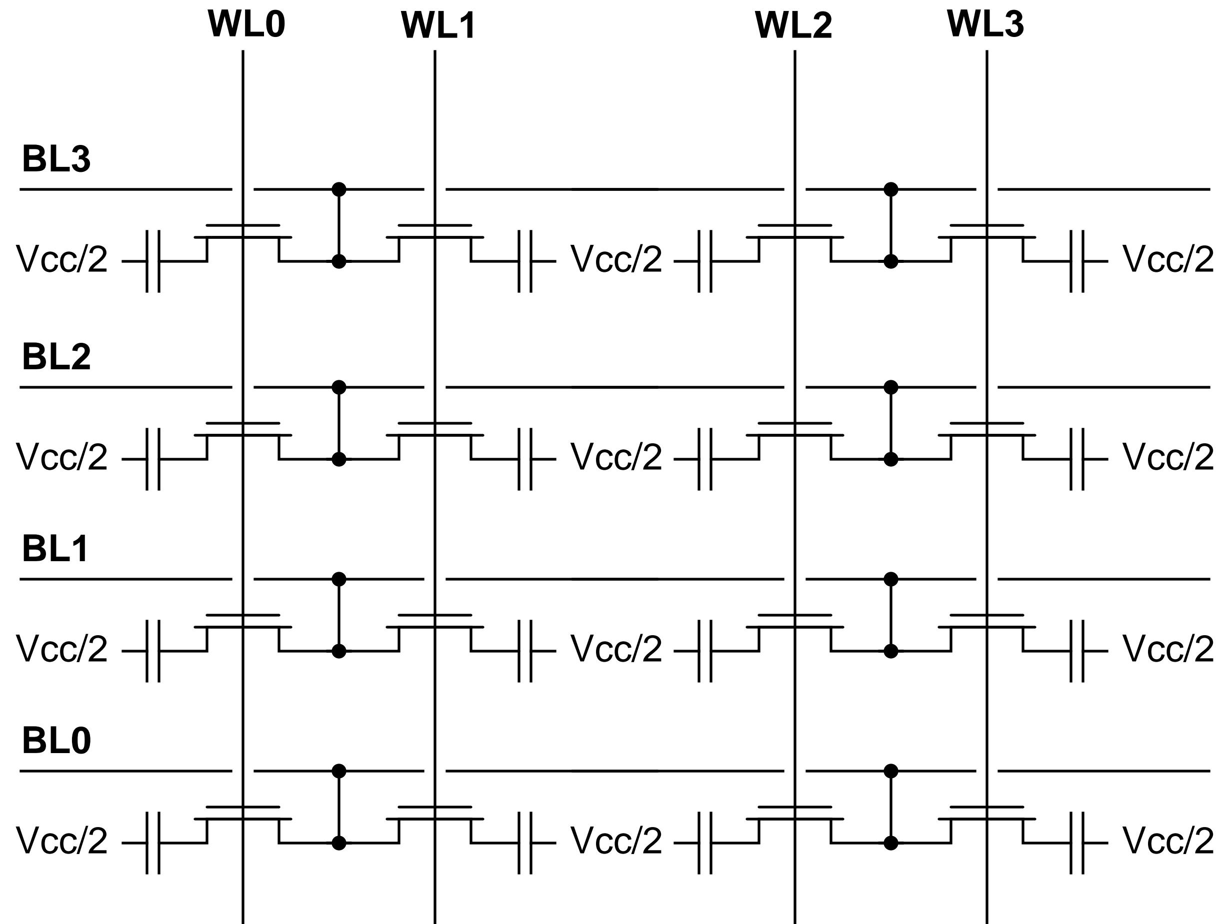
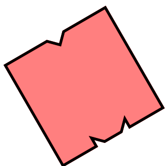
DRAM Array: Open Bitline



- Adjacent cells share connection to bitline
- Note change in orientation (rotated 90º)



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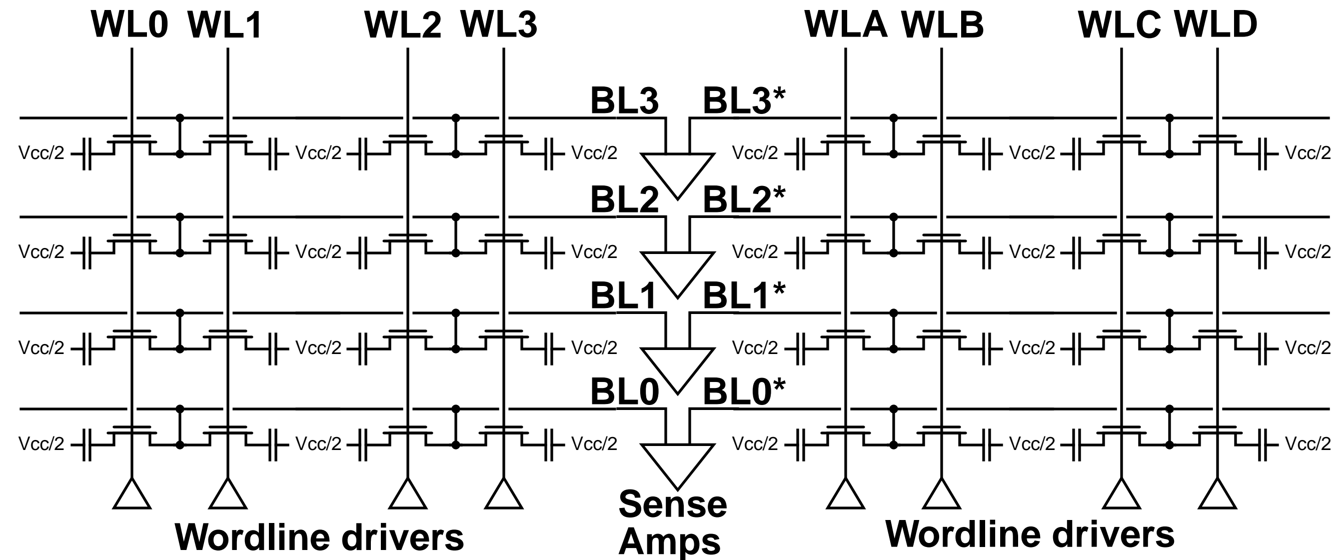
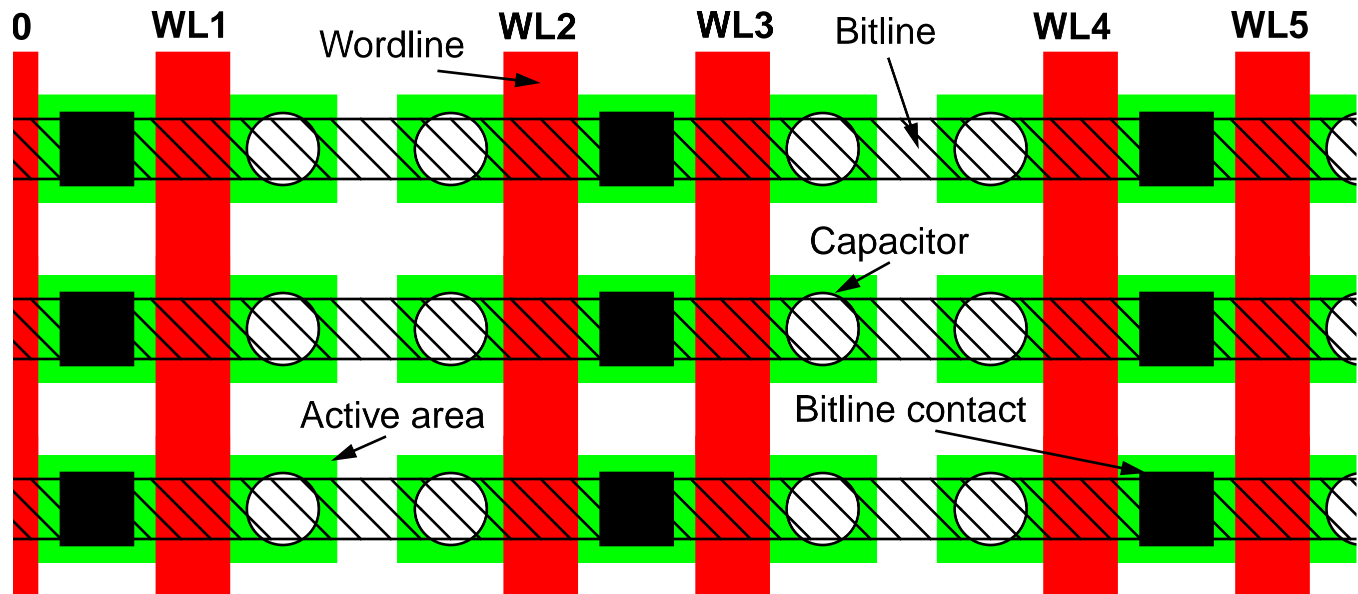
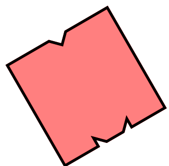
SLIDE 7

Open Bitline Array & Cells







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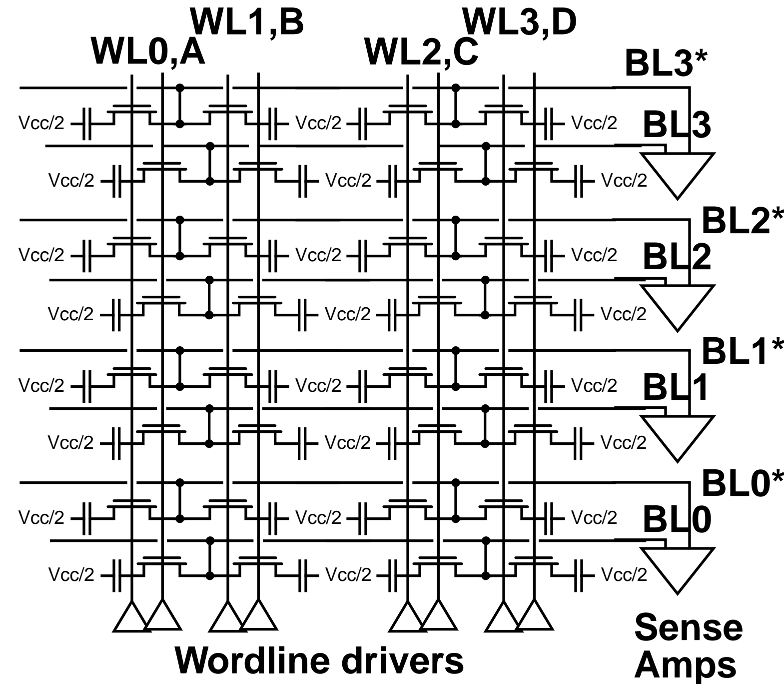
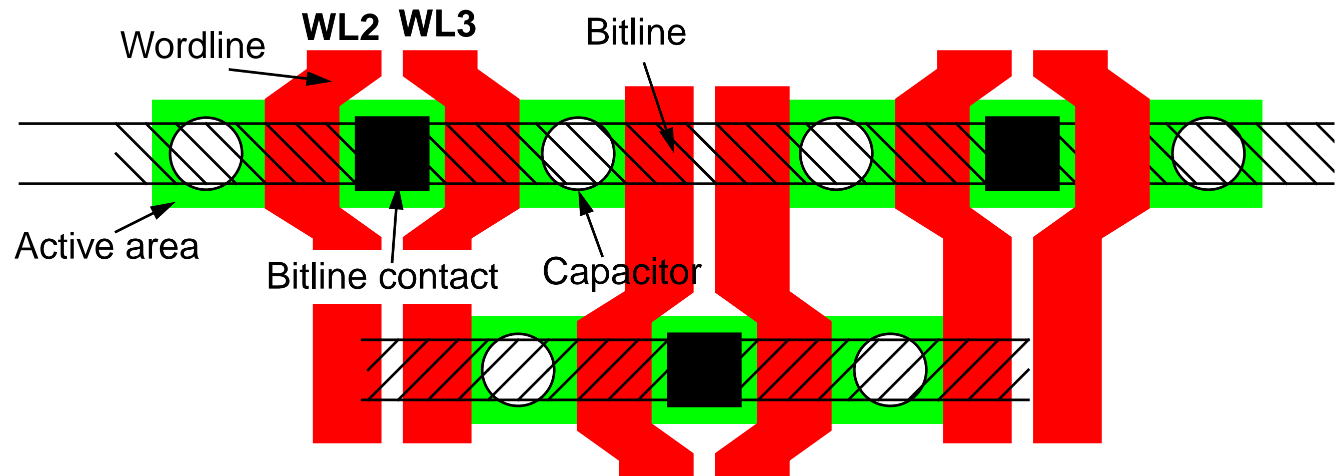
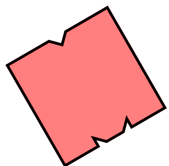
Folded Bitline Array & Cell



Routing BLX and BLX* together improves noise immunity (esp. in conjunction with *bitline twisting …*)





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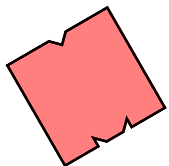
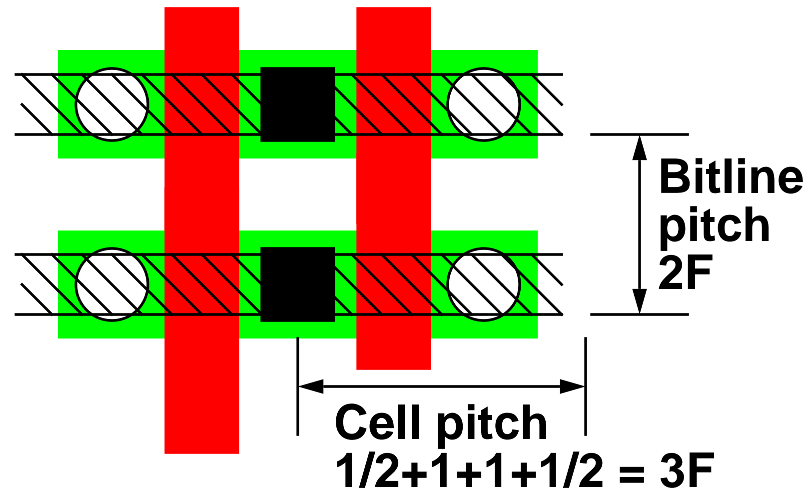
SLIDE 9

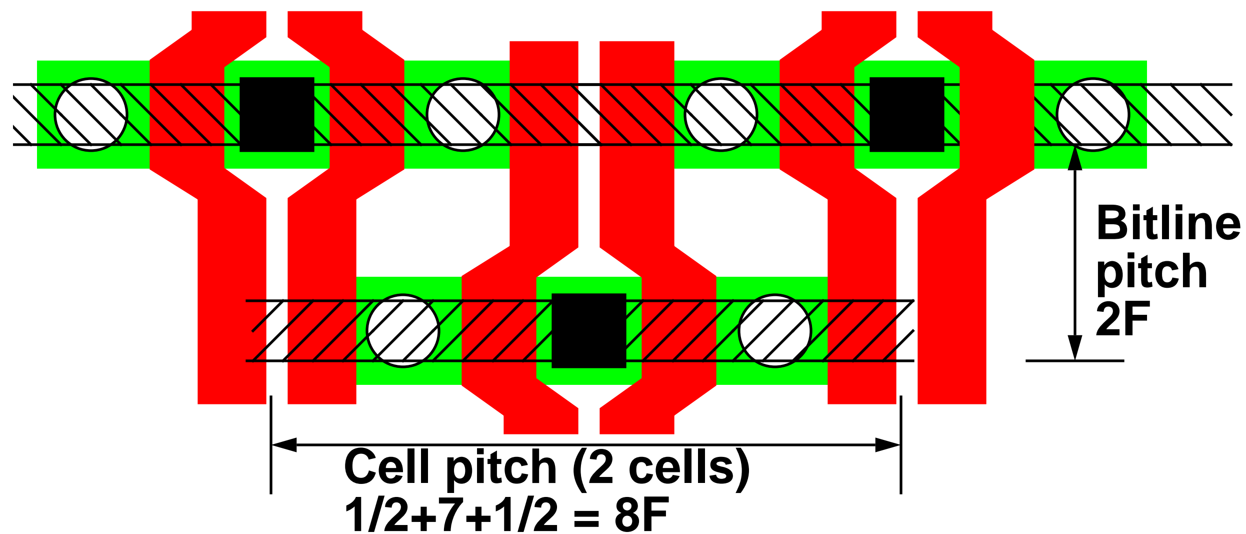


Open vs. Folded Cell Areas



Open bitline cell:
$1F \times 3F = 6F^2$

Folded bitline cell:
$2F \times 4F = 8F^2$



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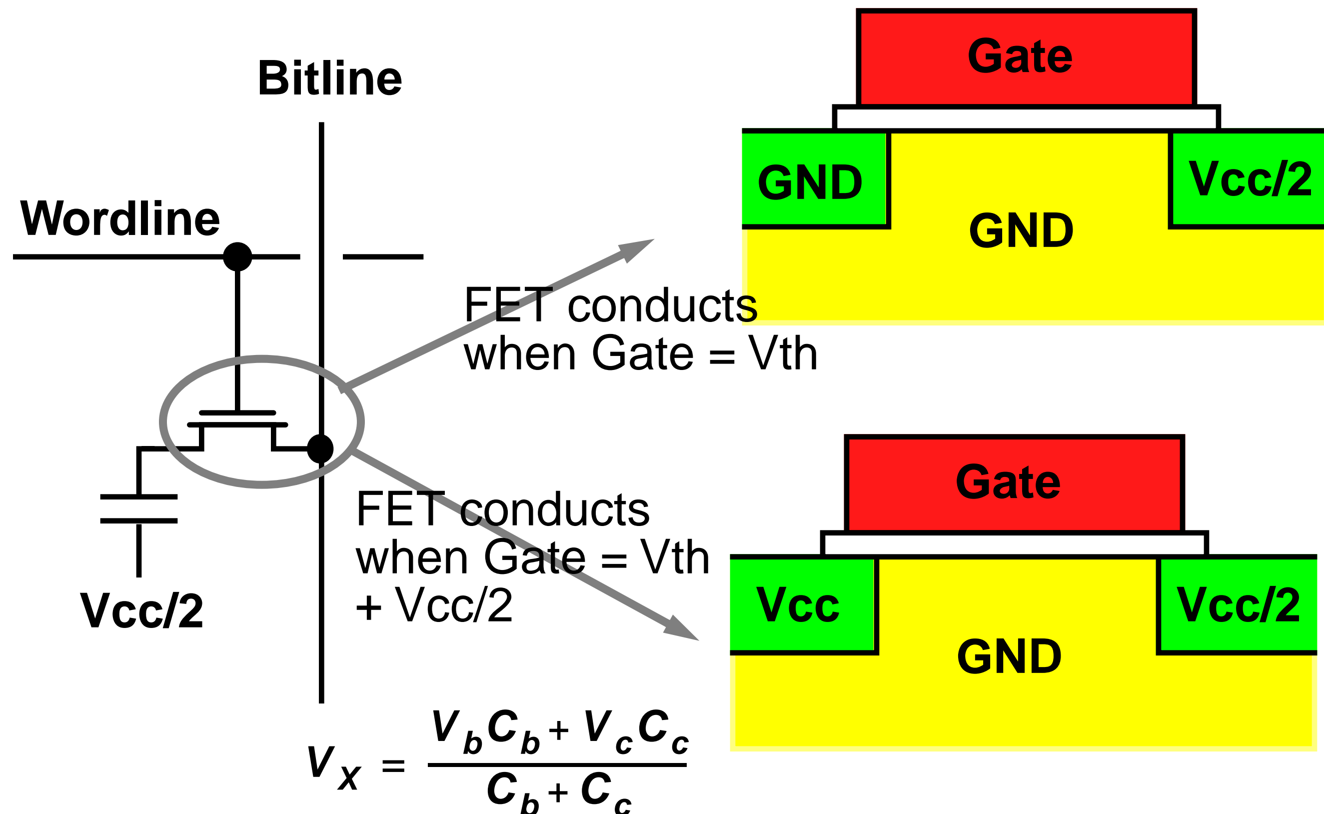
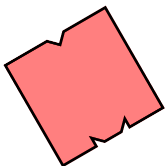
Sensing I

Recall behavior of nFET:

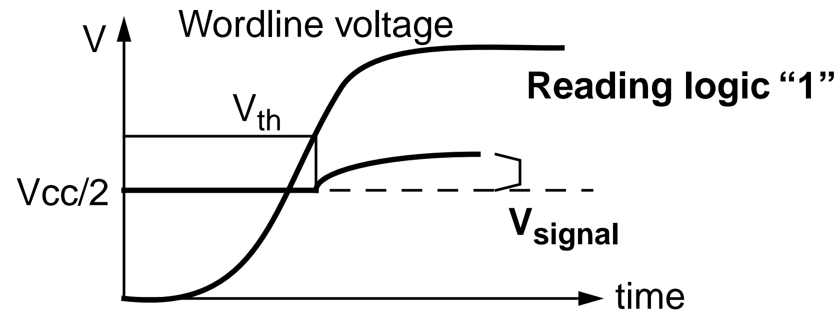


$$V_X = \frac{V_b C_b + V_c C_c}{C_b + C_c}$$

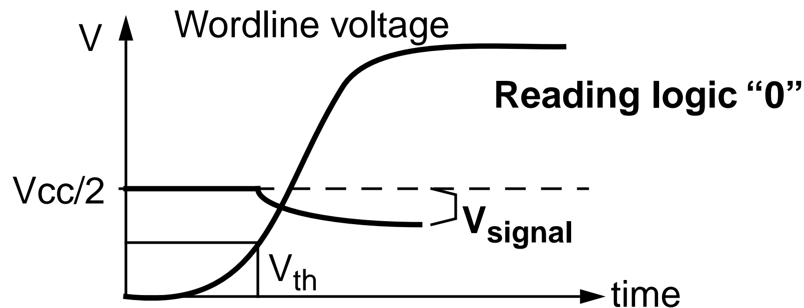
- **Scenario 1: nFET conducts when gate voltage exceeds min{Source,Drain} (GND) by Vth**
- **Scenario 2: nFET conducts when gate voltage exceeds min{Source,Drain} (Vcc/2) by Vth**



Sensing II



$$V_X = \frac{V_b C_b + V_c C_c}{C_b + C_c}$$



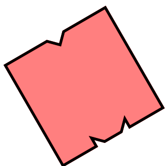
$$V_{signal} = \frac{V_c C_c}{C_b + C_c}$$

Passing Logic 1:

- **Capacitor begins to discharge when wordline exceeds bitline PRECHARGE voltage by Vth**

Passing Logic 0:

- **Capacitor begins to discharge when wordline exceeds Vth**



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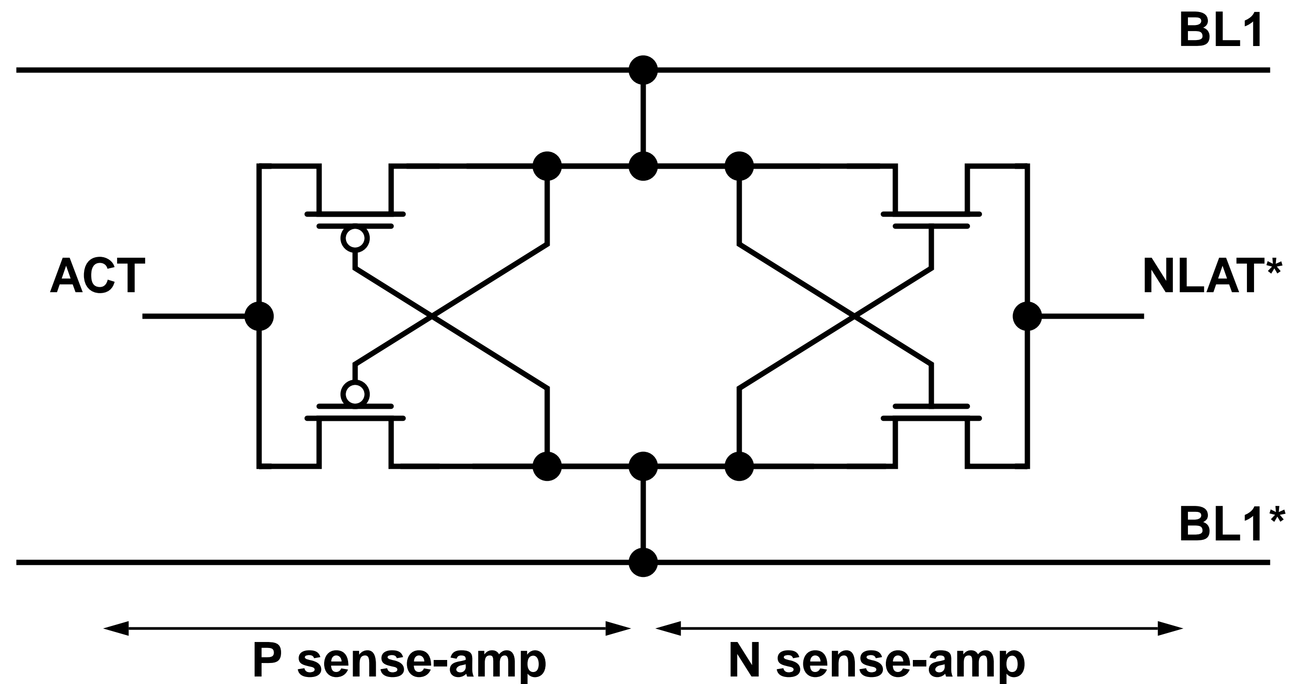
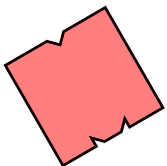
Sense Amplifiers I

Circuit diagram:



- **Initially, ACT at Vss (GND) and NLAT* held at Vcc/2 (both BL1 and BL1* are at Vcc/2 as well)**
- **To read: Wordline pulled to Vcc+Vth, BL1/* changes**
- **To sense: first, NLAT* is pulled towards ground**
- **Then ACT is pulled towards Vcc**



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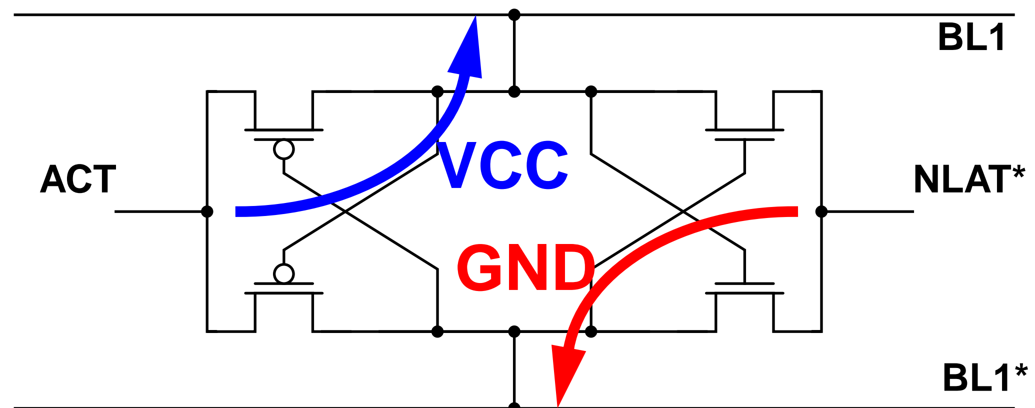
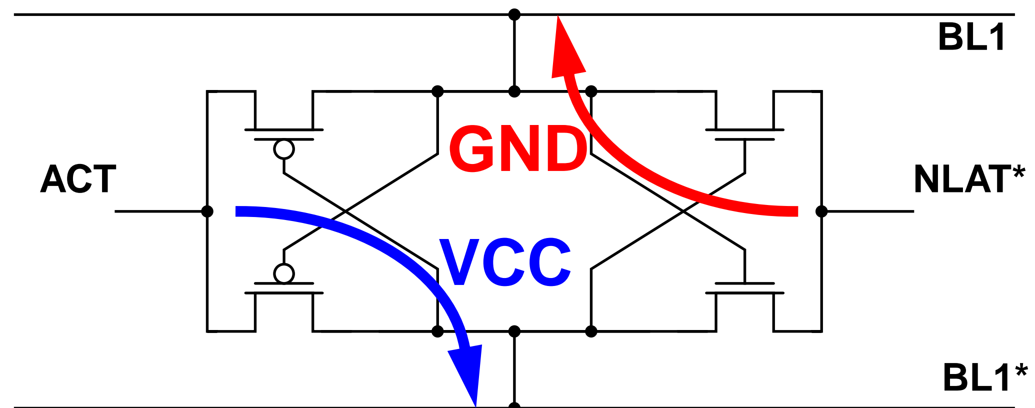
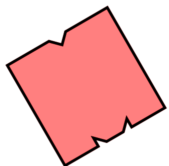
Sense Amplifiers II

Basic idea:



OR





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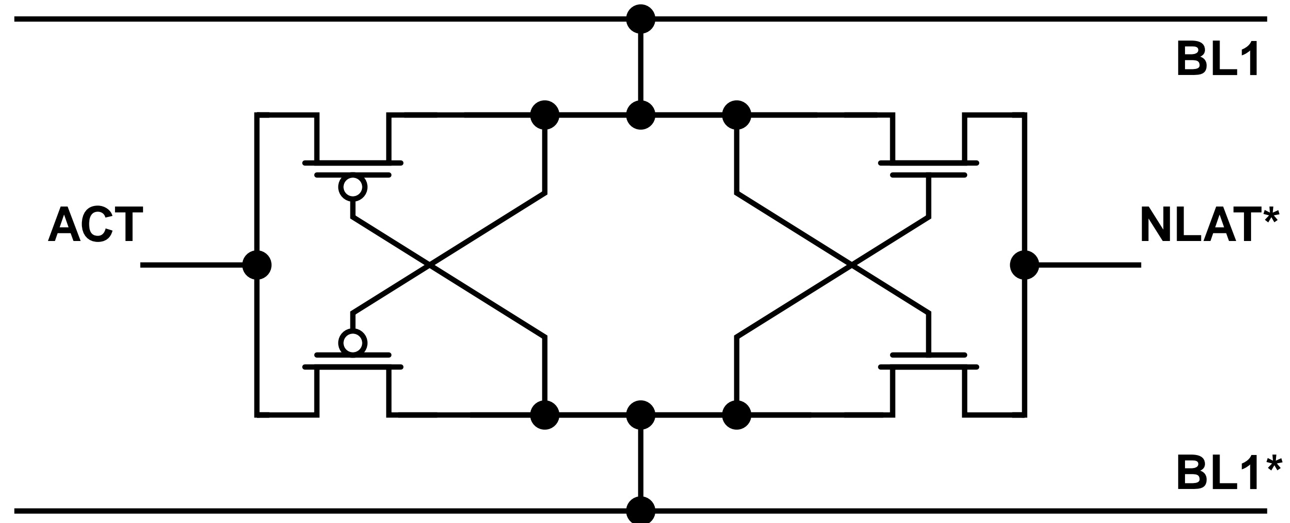
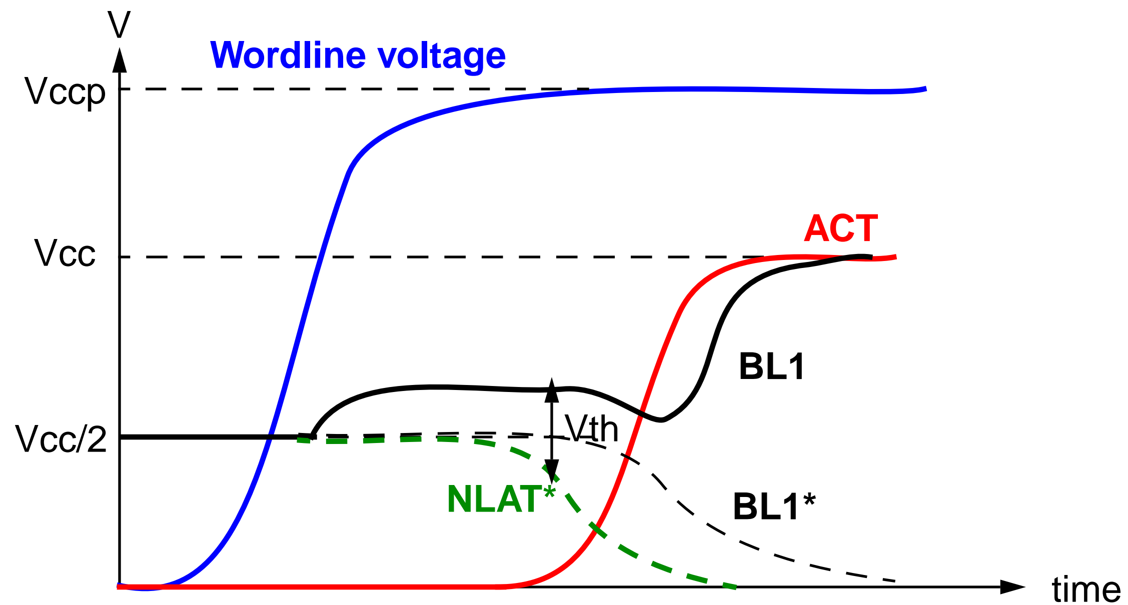
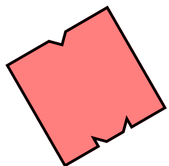
Sense Amplifiers III







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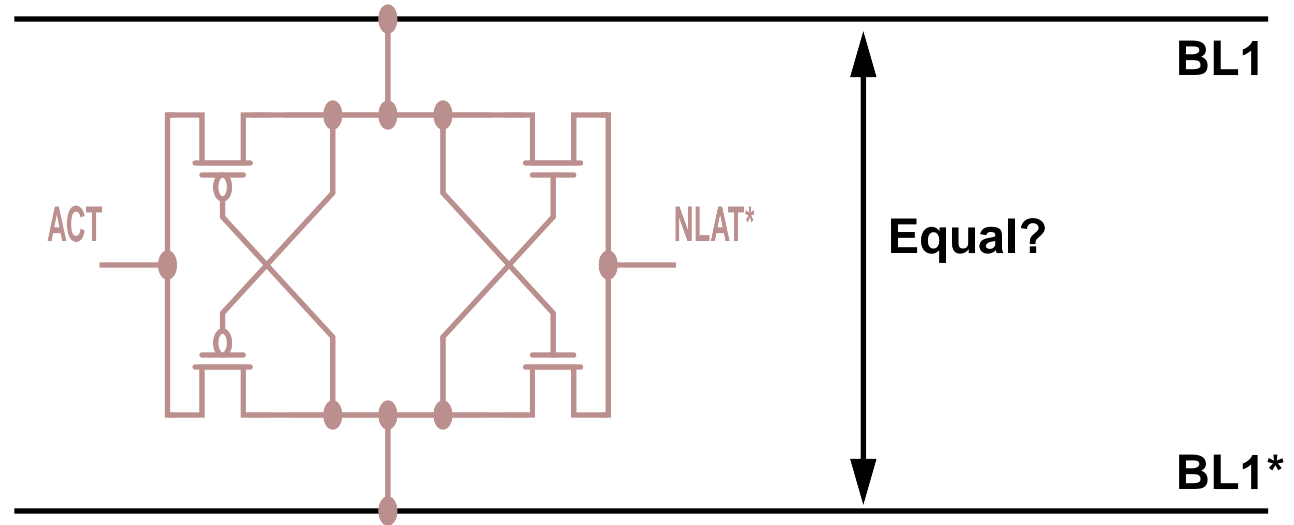
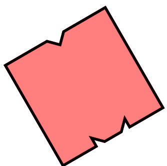
Equilibration I



Textbook’s term: *equalization*



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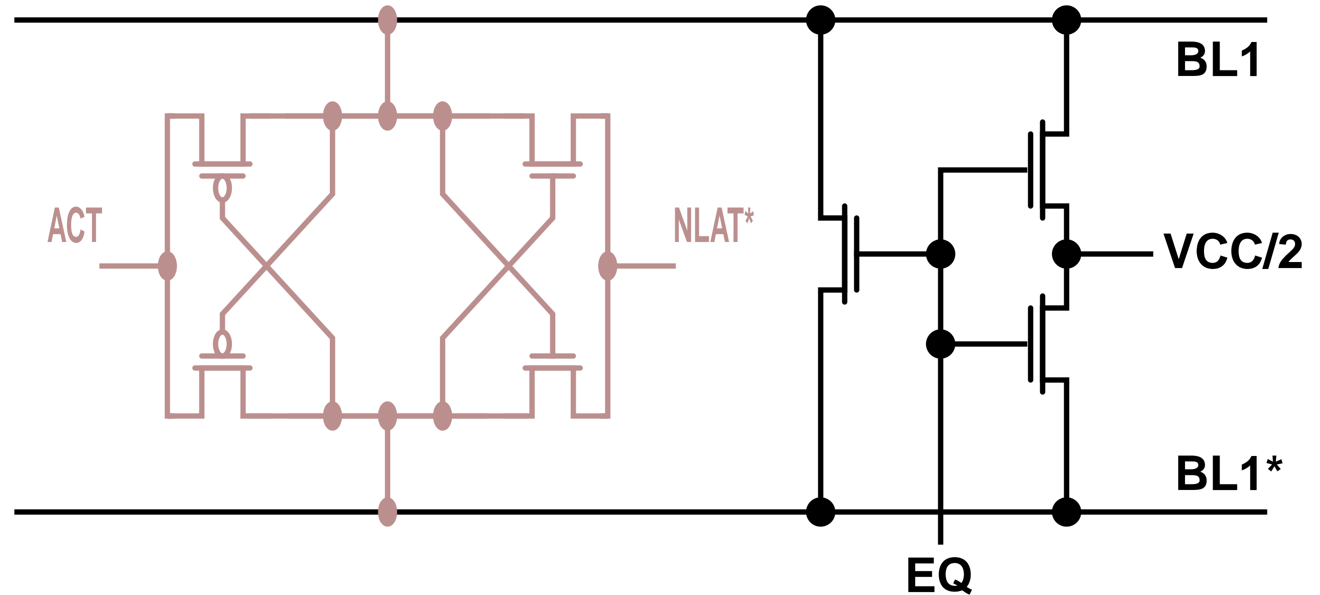
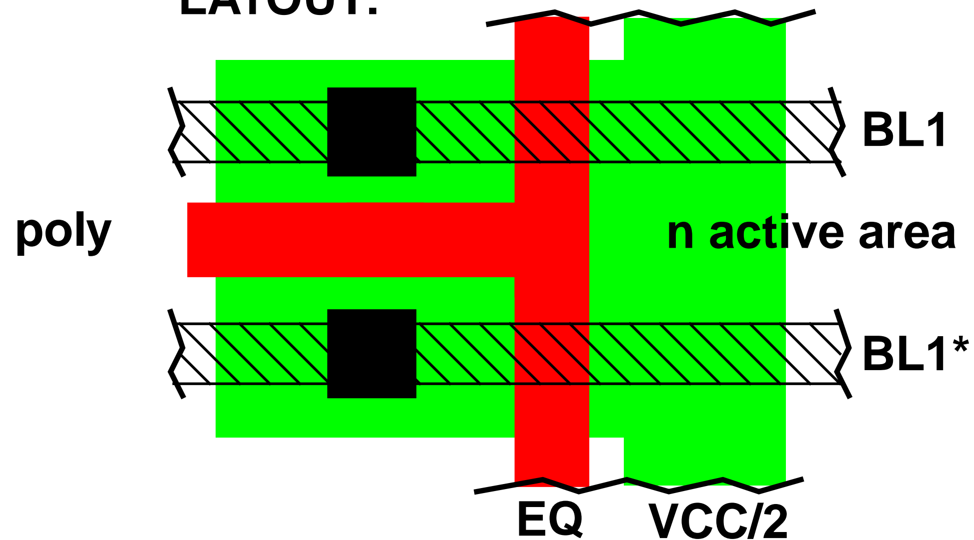
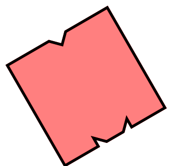
Equilibration II







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Bitline Twisting

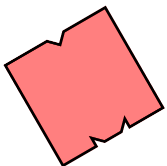
None

Single

Triple

Complex

… this is just a small sample



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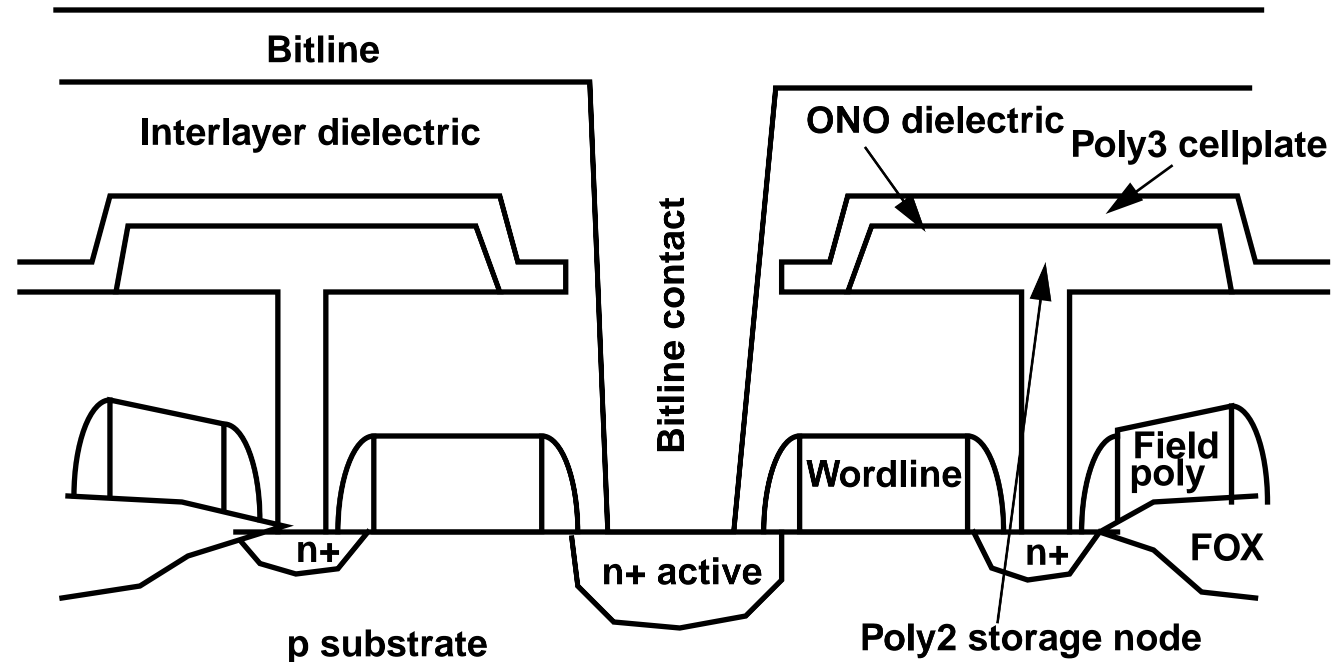
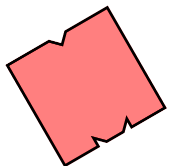
Cells: Buried Capacitor





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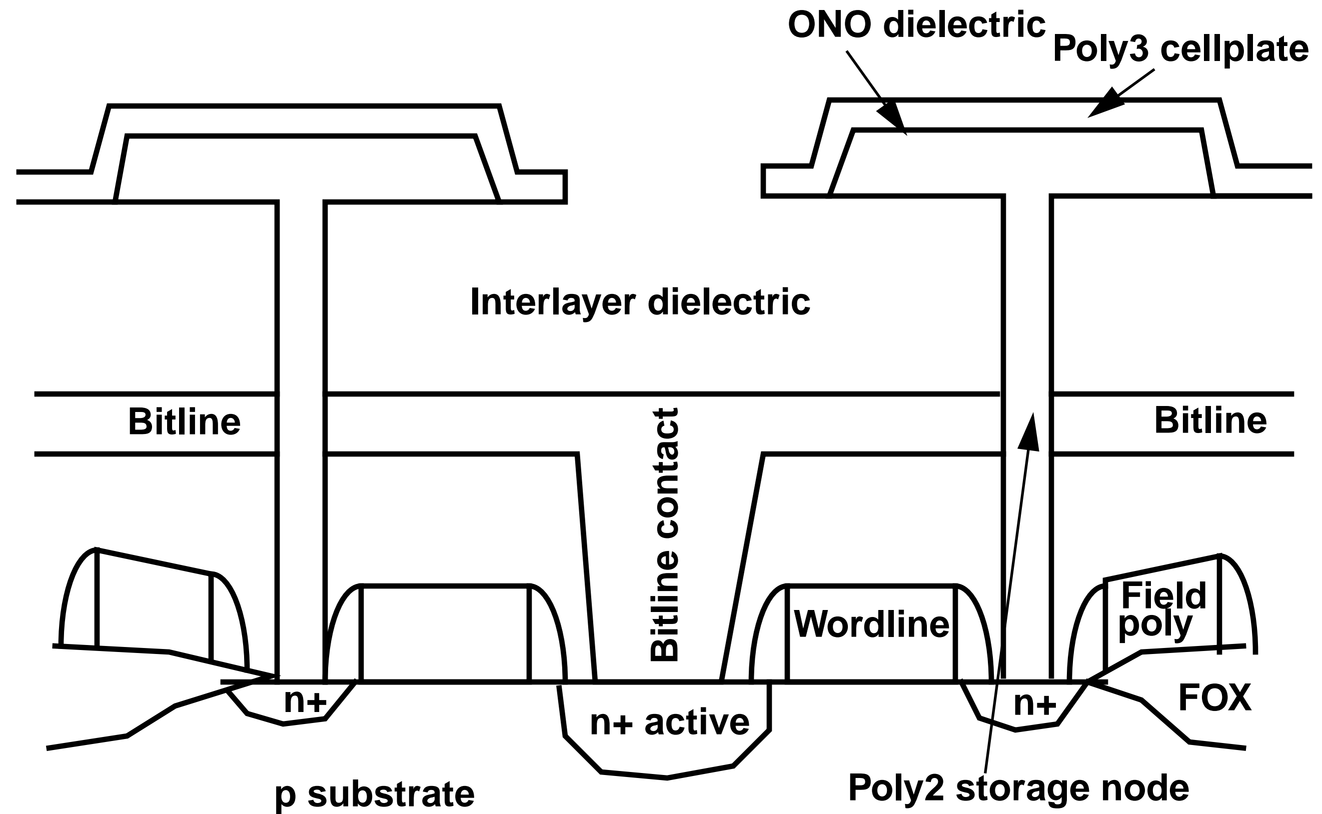
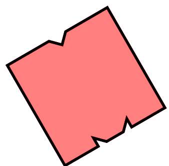
Cells: Buried Bitline/Digitline





Cells: Trench Capacitor

Bitline

Poly strap

Bitline
contact

Wordline

Field
poly

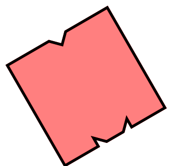
FOX

n+ active

Poly storage node

ONO dielectric

Heavily doped
substrate region



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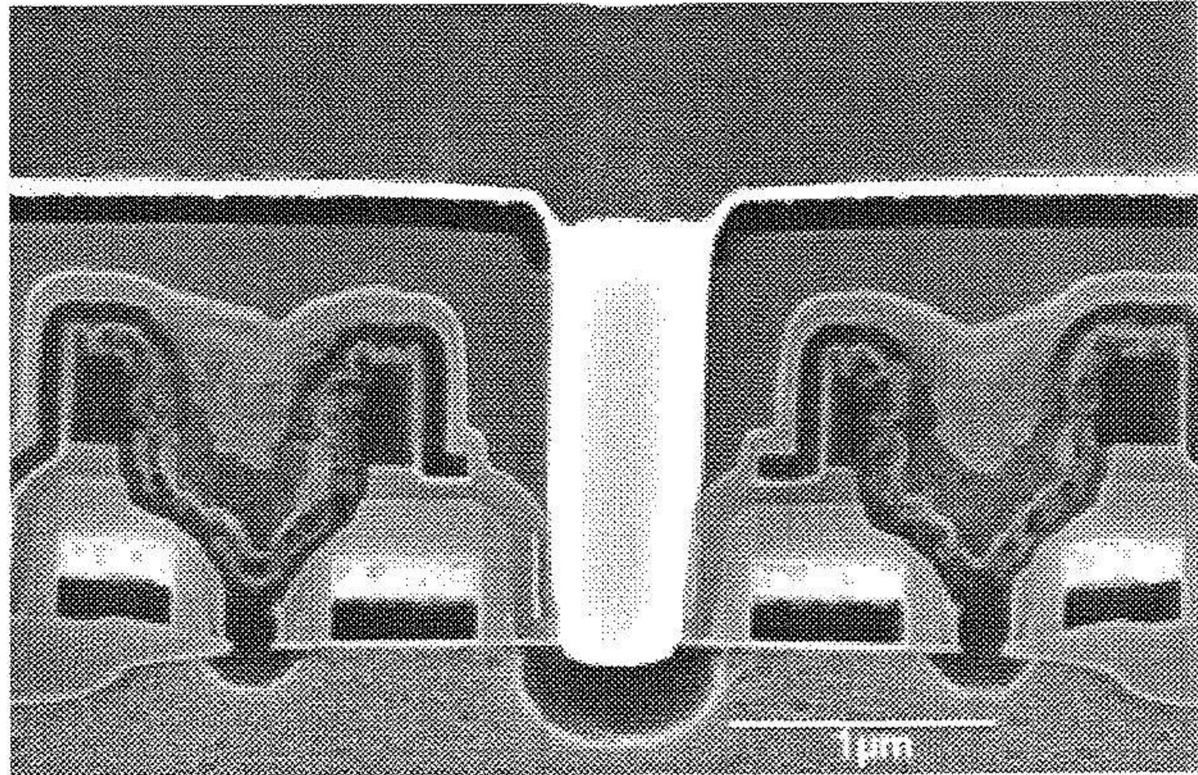
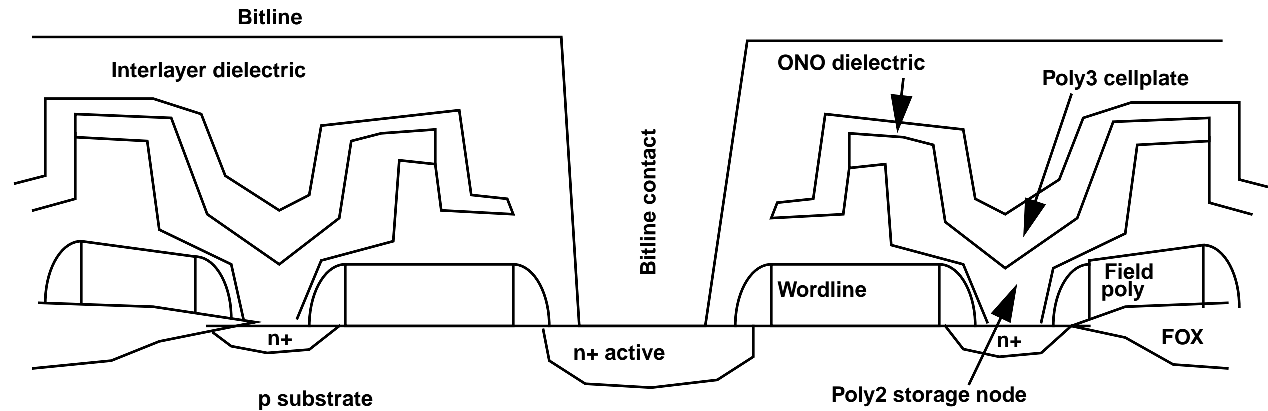
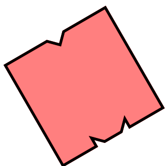
Cells: Buried Capacitor







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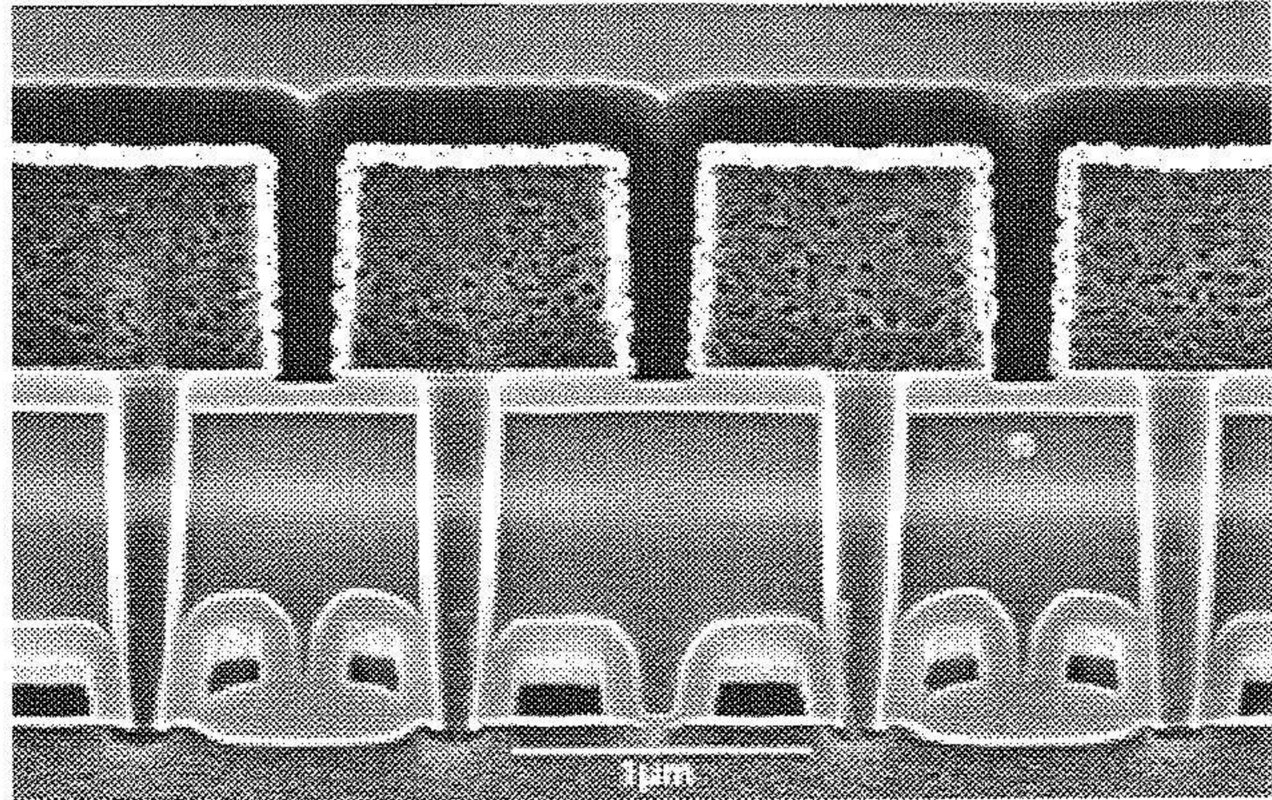
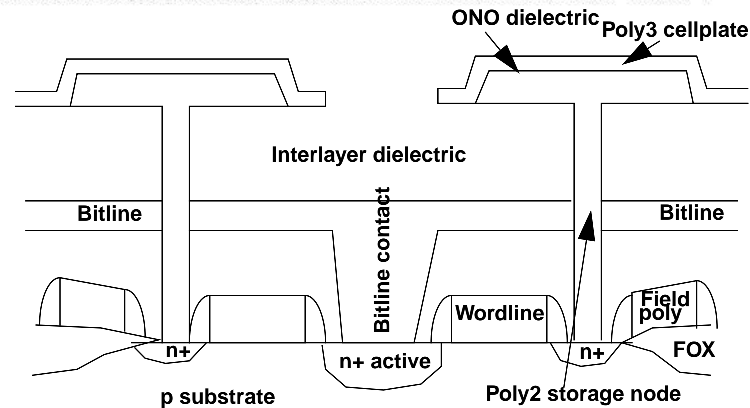
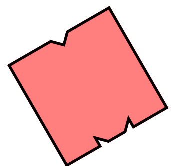
Cells: Buried Bitline/Digitline







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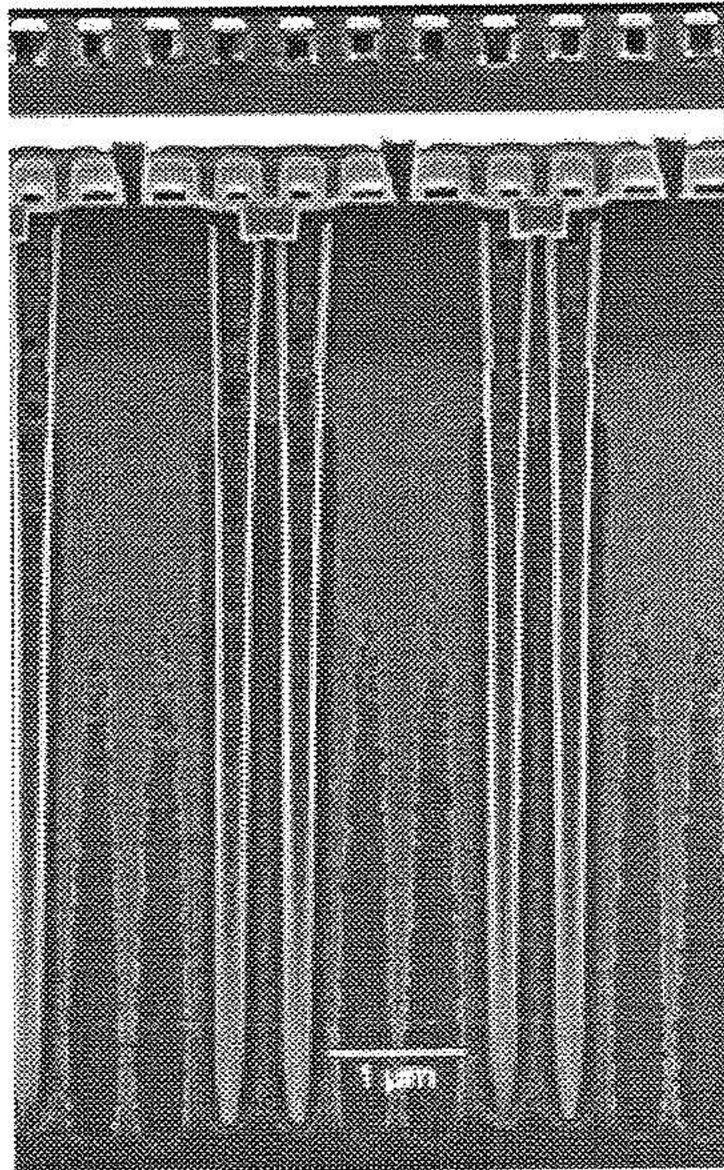
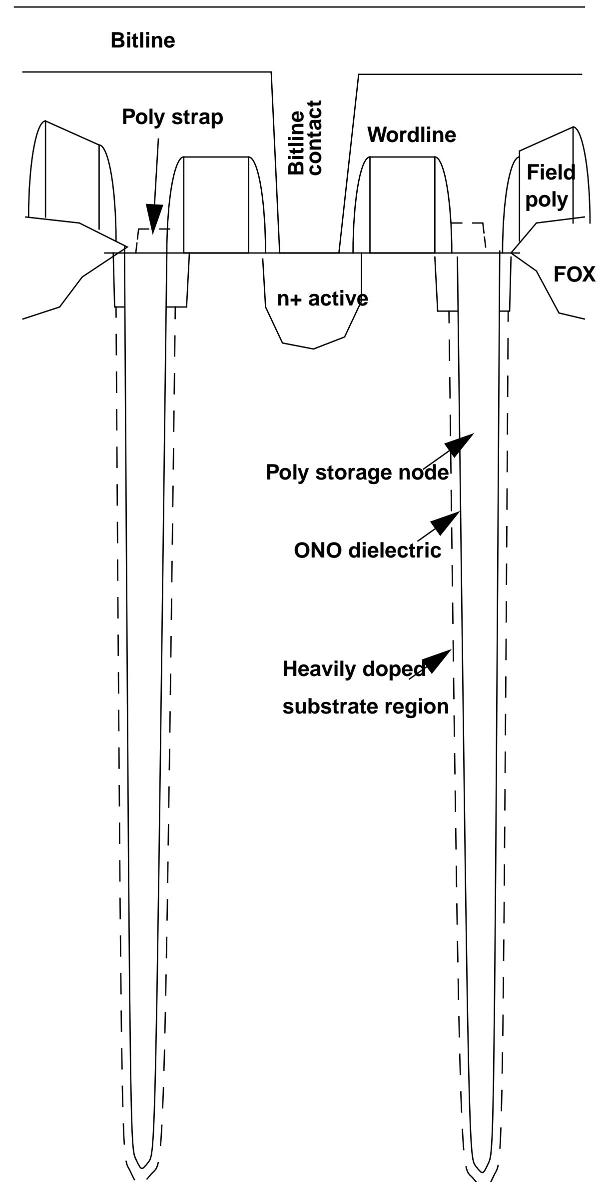
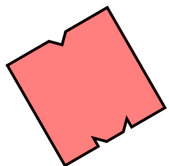
Cells: Trench Capacitor







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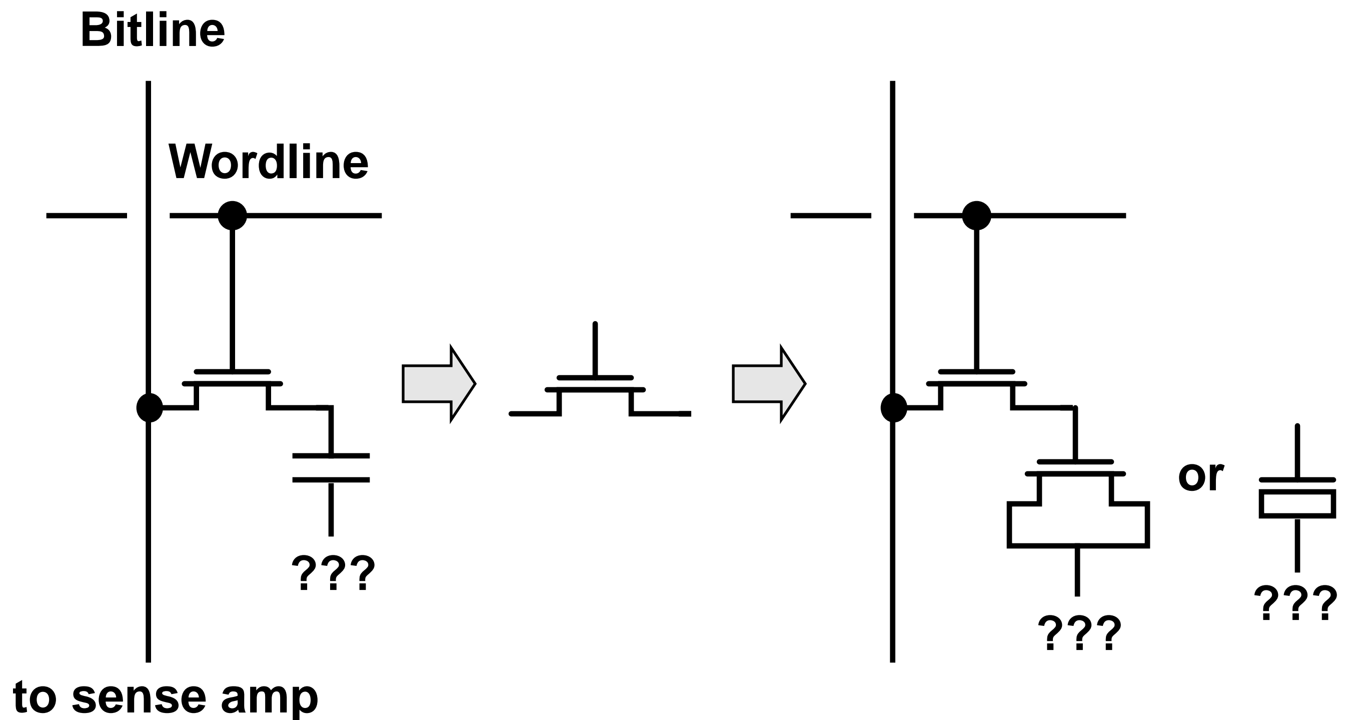
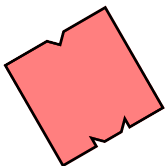
Cells: eDRAM (logic process)



- Basic idea: replace funky capacitor structure (which requires special process technology to produce) with something that looks like logic
- DRAM is now "embedded" into a logic process: on same chip as CPU cores, etc.
- Question: do we still tie far side to VCC/2?



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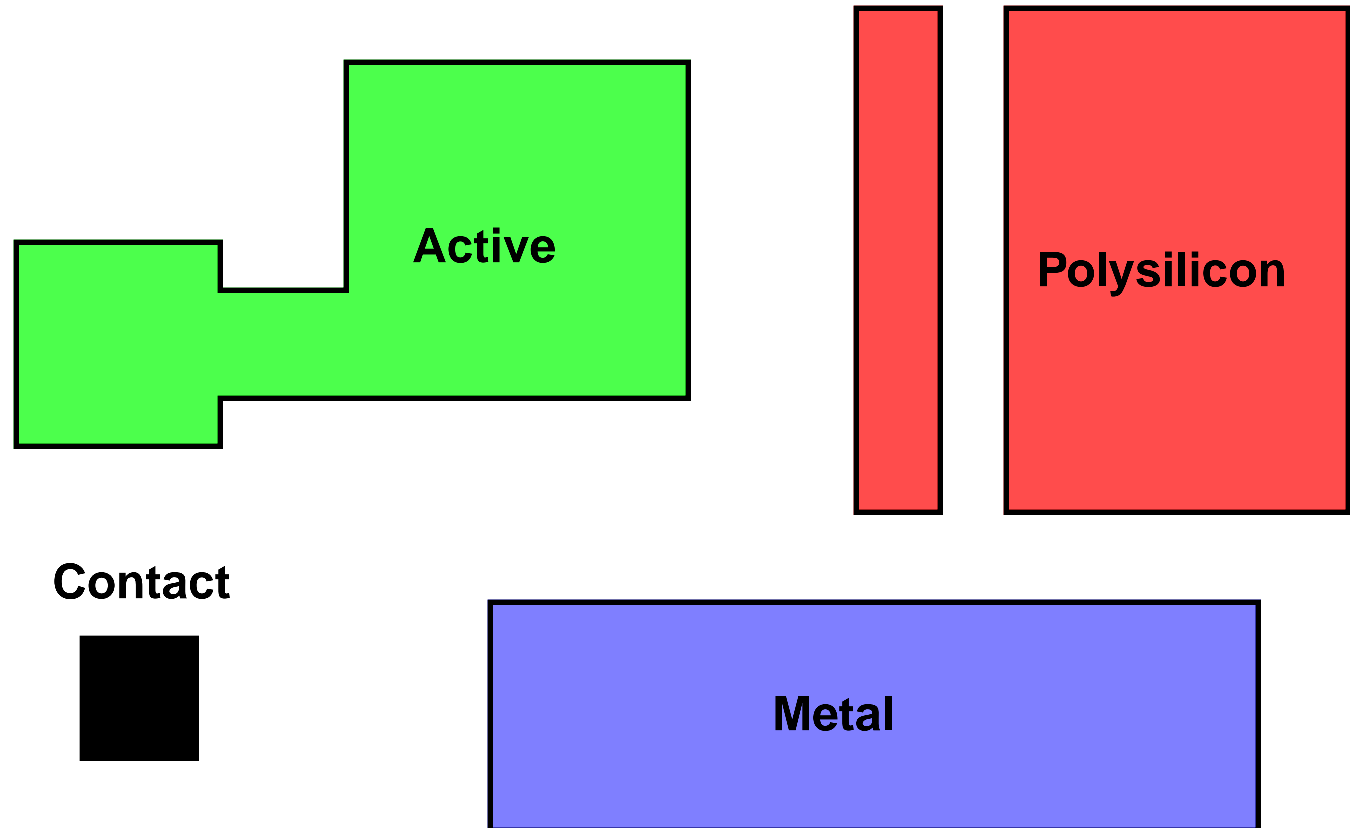
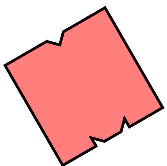


The components



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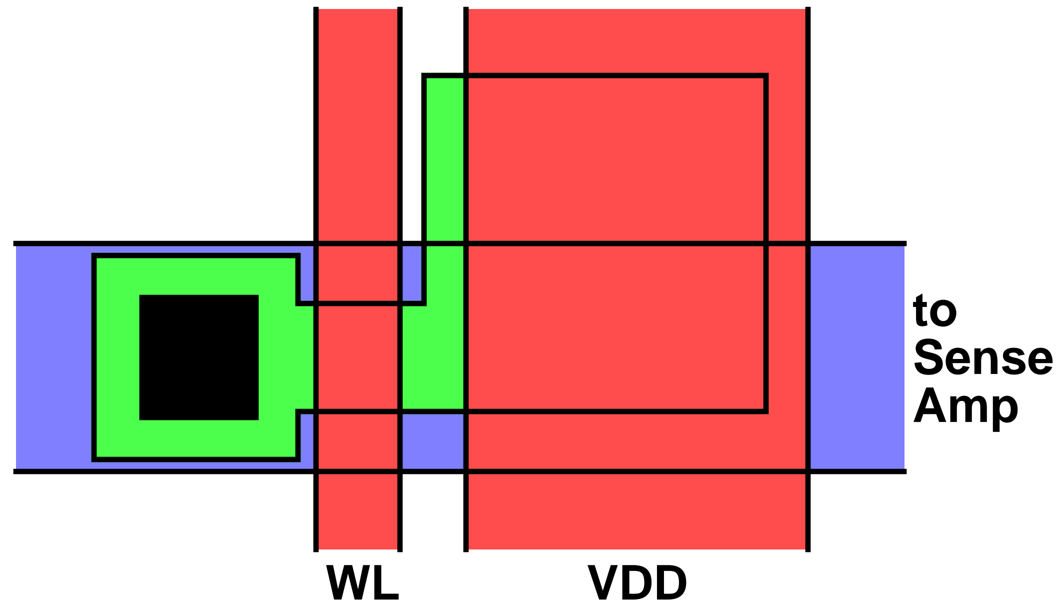
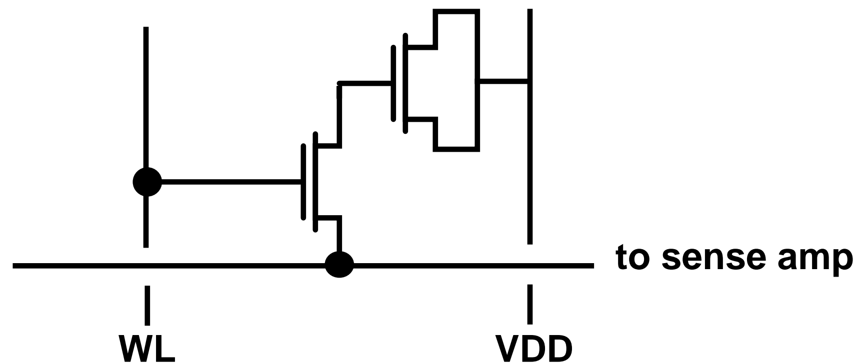
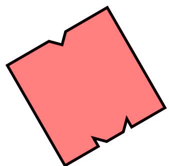
Cells: eDRAM (logic process)





The cell



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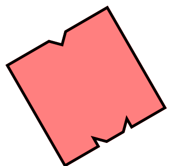

Cells: eDRAM (logic process)

VDD VDD VDD

BL $_{i-1}$

BL $_{i}$

BL $_{i+1}$

BL $_{i+2}$

WL $_{i-1}$ WL $_{i}$ WL $_{i+1}$

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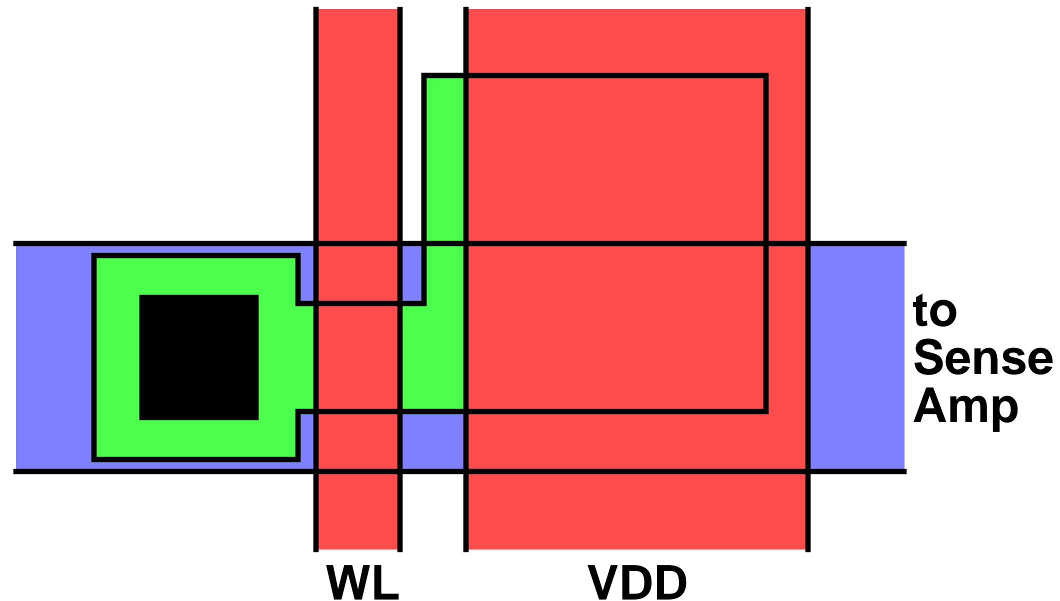
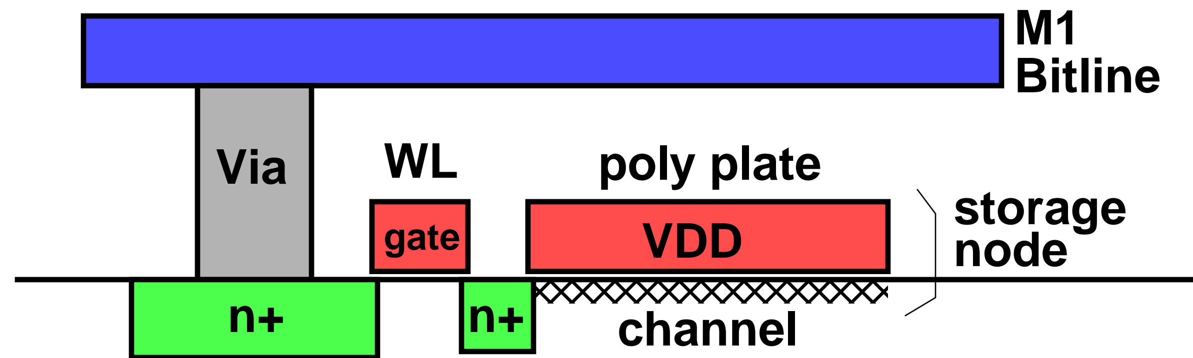
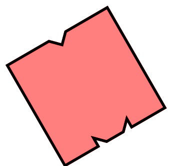
Cells: eDRAM (logic process)





Why is poly plate held at (global) VDD?



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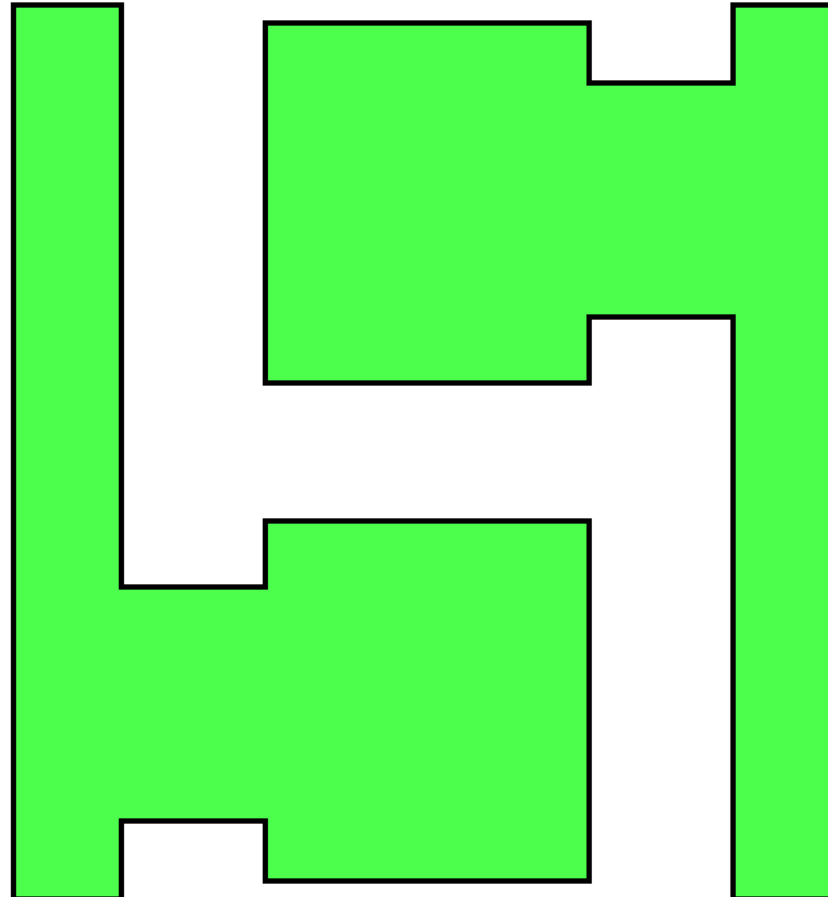
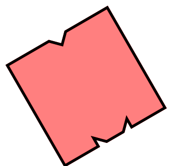
eDRAM: 2-bit cell (CMU)



Active area



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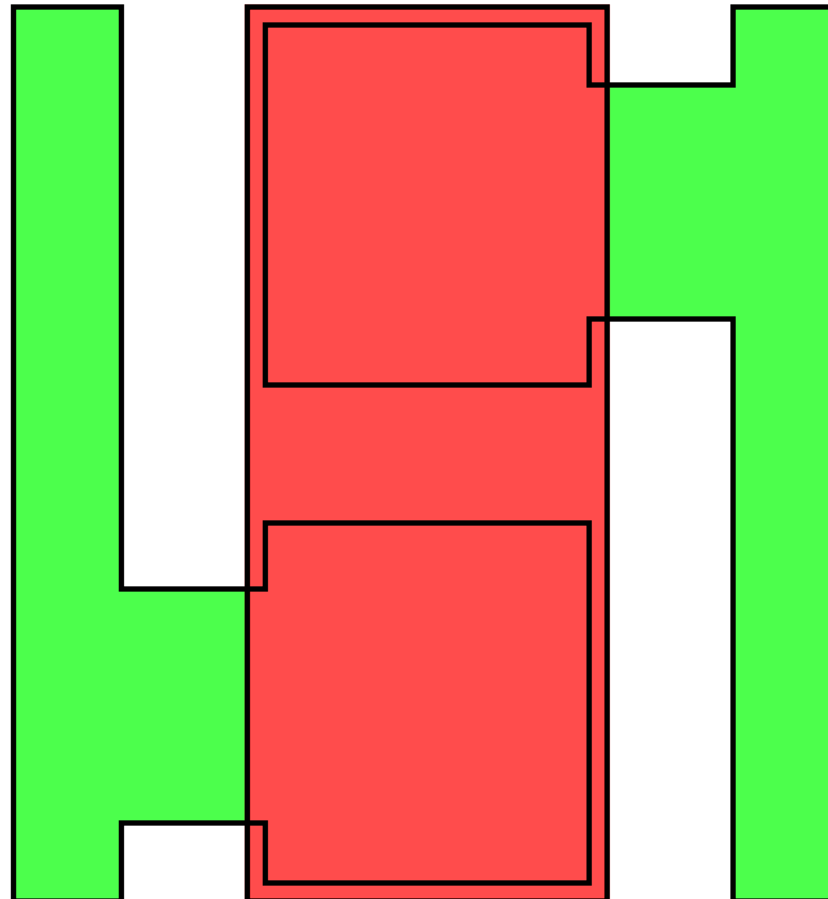
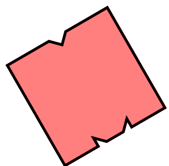
eDRAM: 2-bit cell (CMU)



Poly I



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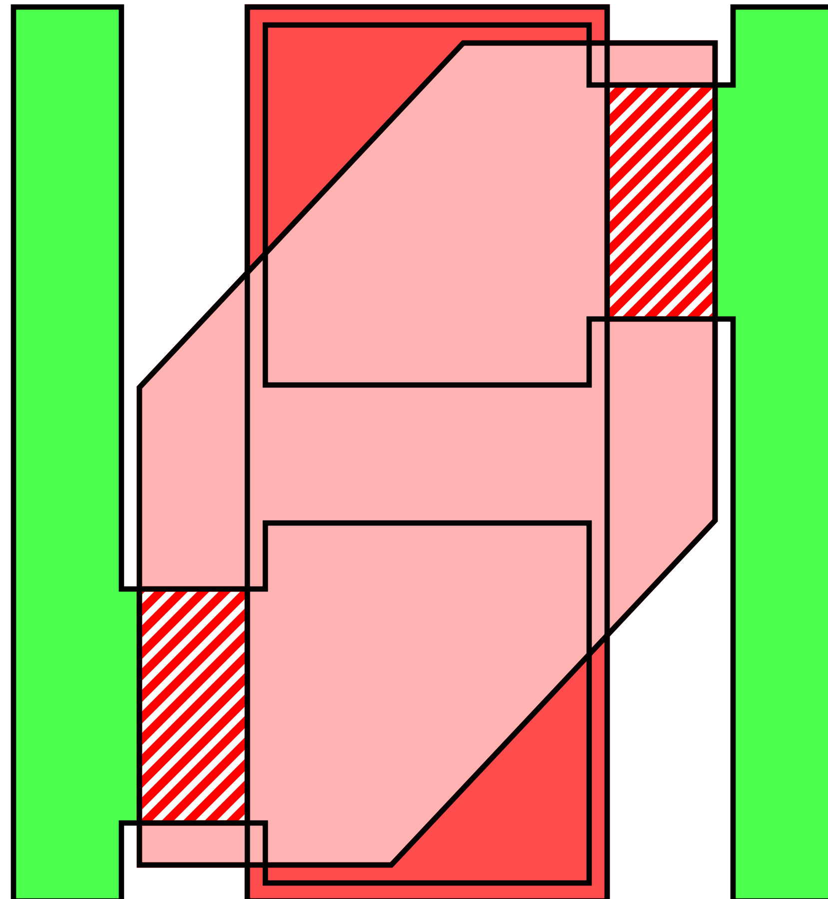
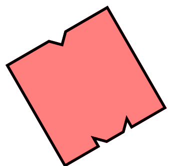
eDRAM: 2-bit cell (CMU)



Poly II



ENEE 359a
Lecture/s 23-25
DRAM Circuits

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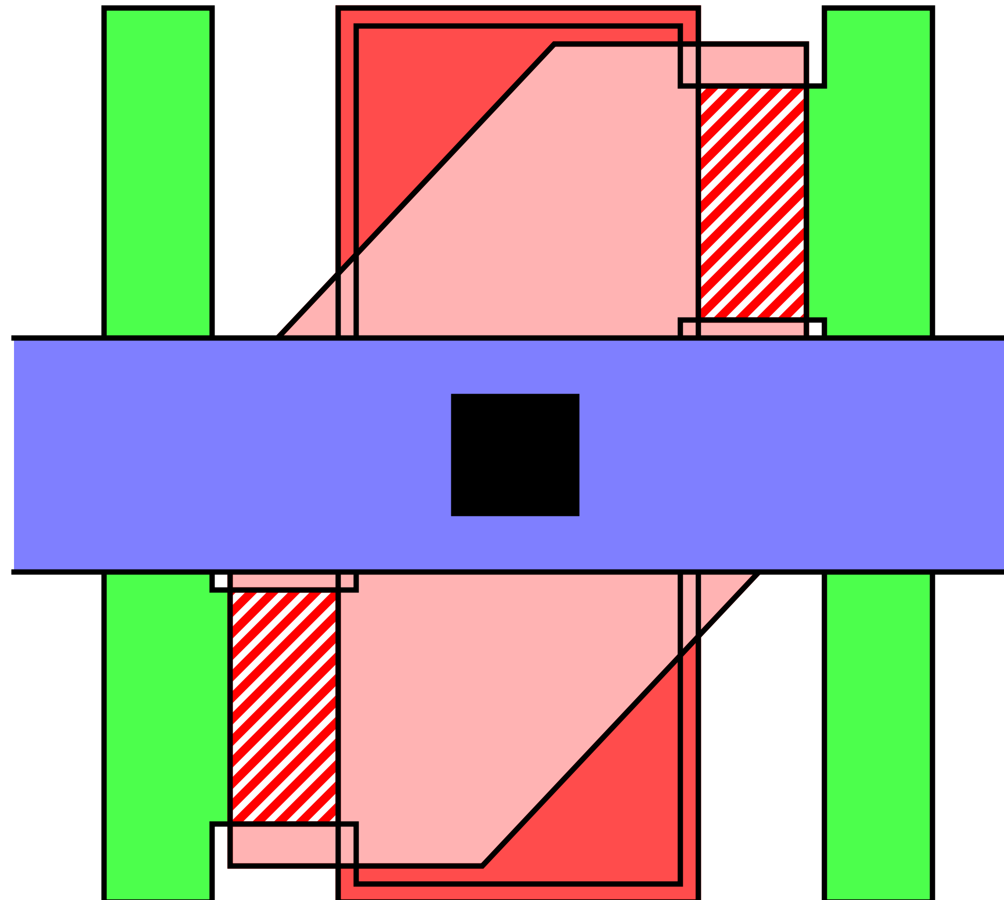
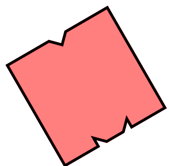
eDRAM: 2-bit cell (CMU)



Via & Metal 1



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eDRAM: 2-bit cell (CMU)