Bruce Jacob

University of
Maryland
ECE Dept.

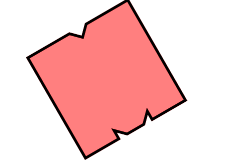
ENEE 359a
Digital VLSI Circuits

P/N Junction, MOS Transistors, CMOS Inverter

Prof. Bruce Jacob

blj@eng.umd.edu

Credit where credit is due:
Slides contain original artwork (© Jacob 2004) as well as material taken liberally from Irwin & Vijay's CSE477 slides (PSU), Schmit & Strojwas's 18-322 slides (CMU), Wolf's slides for *Modern VLSI Design*, and/or Rabaey's slides (UCB).
Device physics: http://hyperphysics.phy-astr.gsu.edu/hbase/solids/sselcn.html



Bruce Jacob

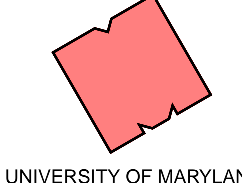
University of
Maryland
ECE Dept.

Overview

- Electrons & holes, bands & band gaps, insulators, conductors, semiconductors
- Silicon crystal lattice & doping
- P/N junction & parasitic capacitance
- n-type/n-channel MOSFET
- Timing analysis of MOSFET, capacitance
- Body effect, series-connected FETs
- CMOS inverter: timing, switching threshold, transistor sizing
- Dynamic behavior (preview)

Bruce Jacob

University of
Maryland
ECE Dept.



What Is Conductivity?

Perspective from Band Theory of Solids:

Large band gap (not “Gap Band”) between valence and conduction bands in insulator material suggests that, at ordinary temperatures, no electrons can reach conduction band (i.e. material won’t conduct)

In semiconductors, the band gap is small enough that thermal energy can bridge gap for small fraction of electrons.

In conductors, there is no band gap (conduction and valence bands overlap).

Energy of electrons

Conduction Band

INSULATOR

SEMICONDUCTOR

CONDUCTOR

Fermi level

Fermi level

Conduction Band

Conduction Band

Valence Band

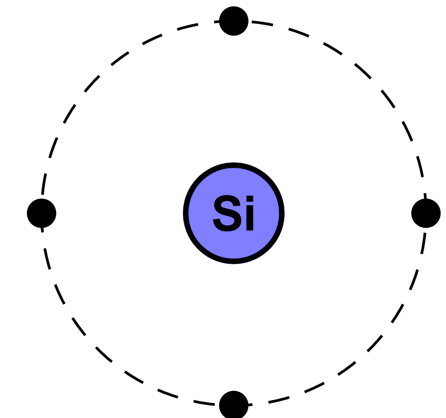
Valence Band

Valence Band

Bruce Jacob

University of
Maryland
ECE Dept.

Silicon, Specifically



14 protons in nucleus
4 valence electrons

Bruce Jacob

University of
Maryland
ECE Dept.

Silicon, Specifically

Bruce Jacob

University of
Maryland
ECE Dept.

Silicon, Specifically

Silicon Lattice (artistic license exploited)

Silicon, Specifically

Silicon Lattice — It *is* a semiconductor

Bruce Jacob

University of
Maryland
ECE Dept.

Silicon, Specifically

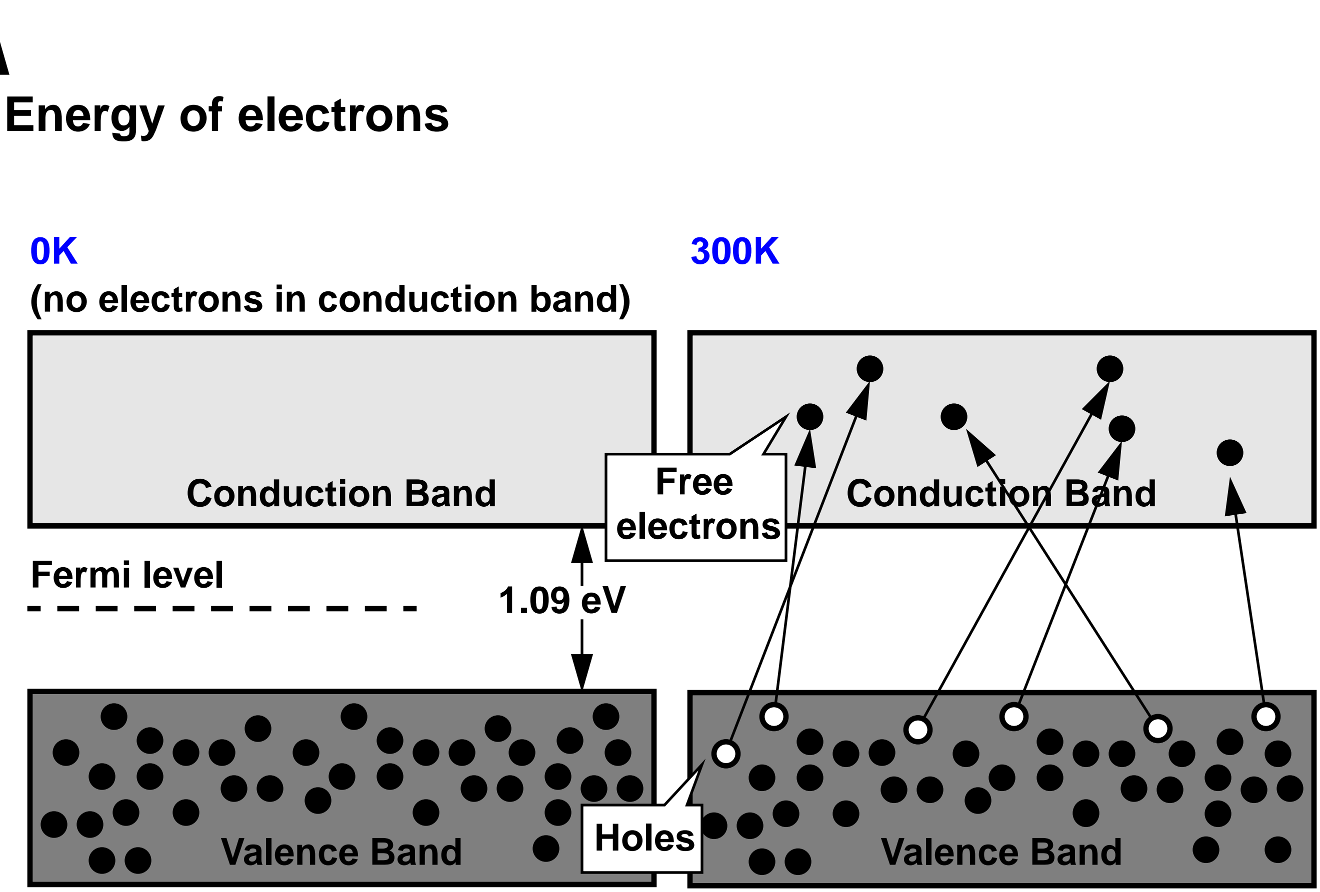
Semiconductor current: electron/hole flow

Bruce Jacob

University of
Maryland
ECE Dept.

Silicon, Specifically

Perspective from Band Theory of Solids:



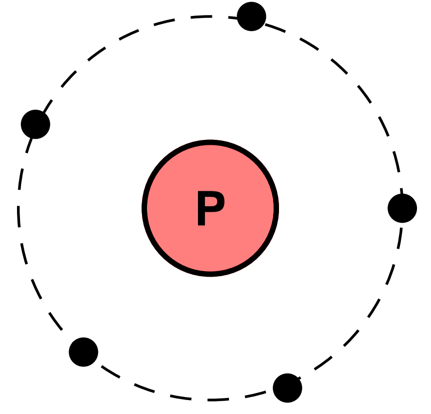
- **Conductivity is non-zero; mobile electrons/holes in conduction/valence band; can be increased w/ doping**

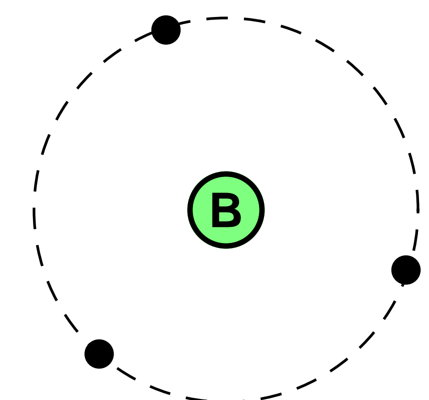
Bruce Jacob

University of
Maryland
ECE Dept.

Silicon, Specifically

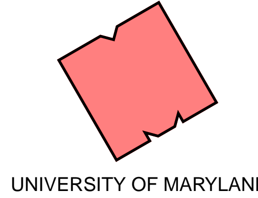
Doping: small % of foreign atoms in lattice





Breaks up regular lattice, produces dramatic changes in electrical properties

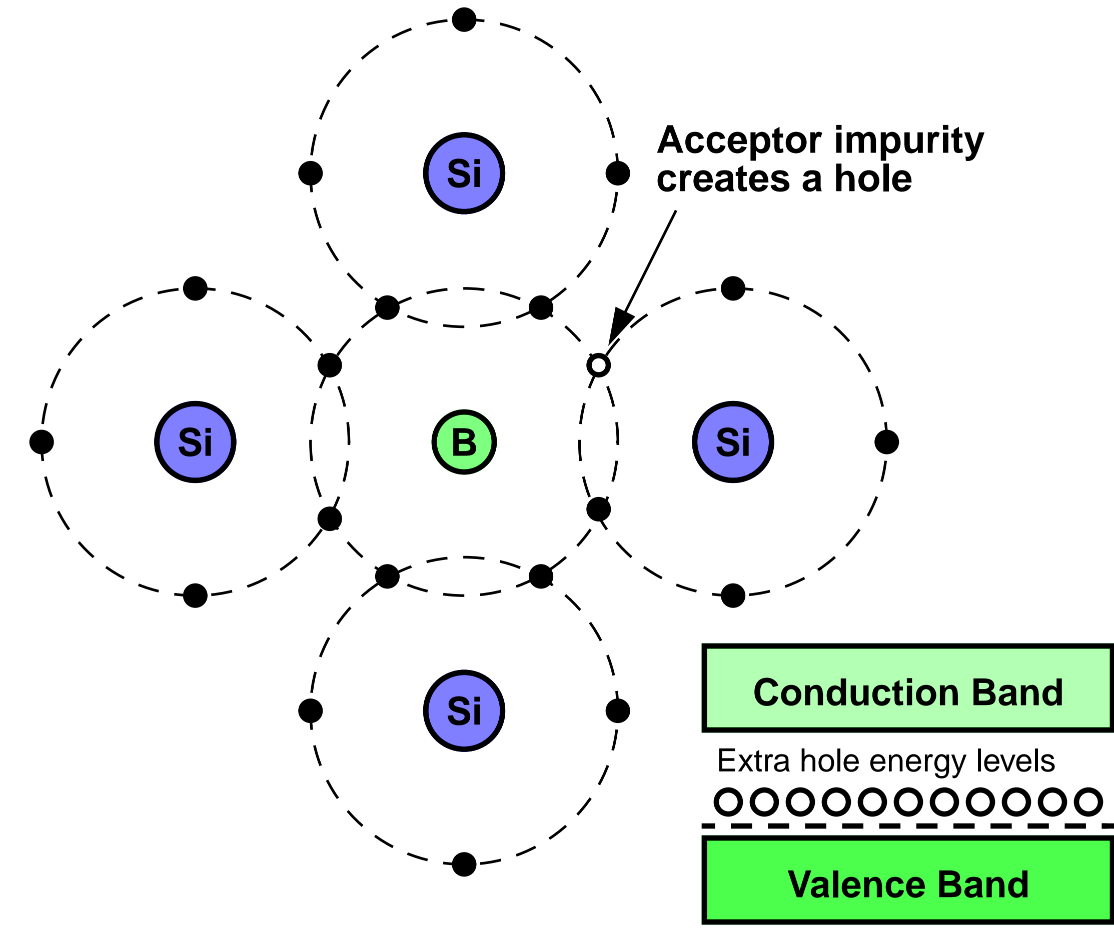
- **Donors: pentavalent impurities (5 valence electrons) produce n-type semiconductors by adding electrons. E.g. antimony, arsenic, phosphorus**
- **Acceptors: trivalent impurities (3 valence electrons) produce p-type semiconductors by adding electron deficiencies (“holes”). E.g. boron, aluminum, gallium**



Bruce Jacob

University of
Maryland
ECE Dept.

P-Type Semiconductor

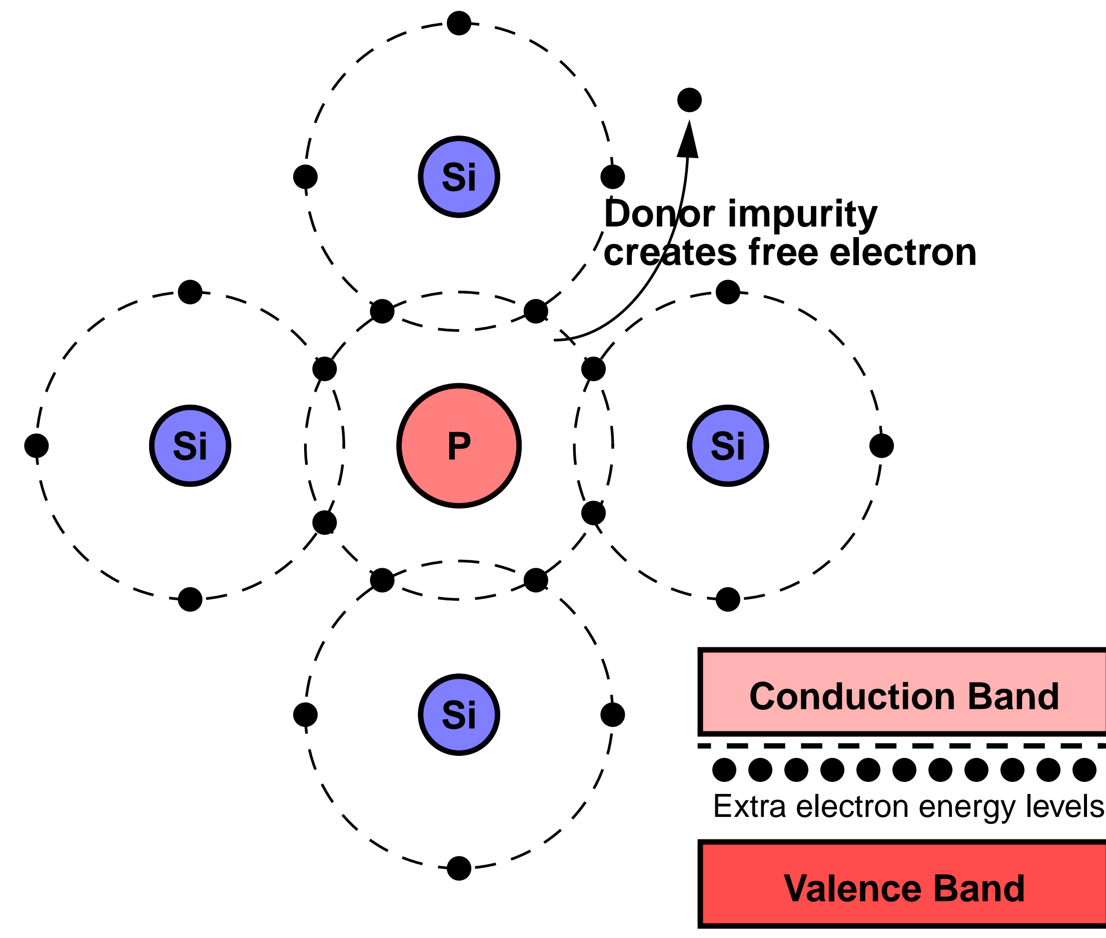


Addition of acceptor impurities contributes hole energy levels low in the semiconductor band gap so that electrons can be easily excited from the valence band into these levels, leaving mobile holes in the valence band. This shifts the effective Fermi level to a point about halfway between the acceptor levels and the valence band. Electrons can be elevated from the valence band to the holes in the band gap with the energy provided by an applied voltage. Since electrons can be exchanged between the holes, the holes are said to be mobile. Holes are said to be the “majority carriers” for current flow in a p-type semiconductor.

Bruce Jacob

University of
Maryland
ECE Dept.

N-Type Semiconductor



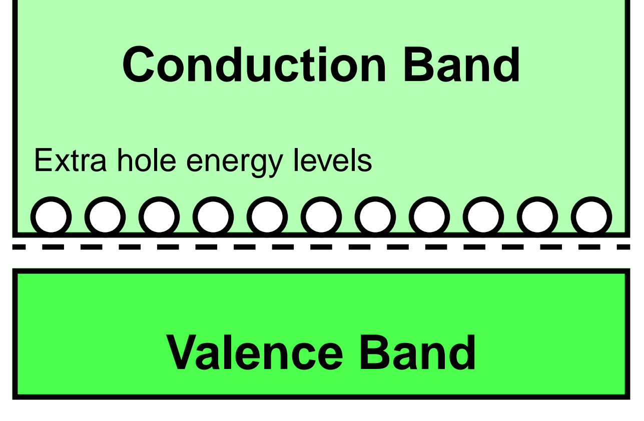
Addition of donor impurities contributes electron energy levels high in the semiconductor band gap so that electrons can be easily excited into the conduction band. This shifts the Fermi level to a point about halfway between the donor levels and the conduction band. Electrons can be elevated to the conduction band with the energy provided by an applied voltage and move through the material. Electrons are said to be the “majority carriers” for current flow in an n-type semiconductor.

Bruce Jacob

University of
Maryland
ECE Dept.

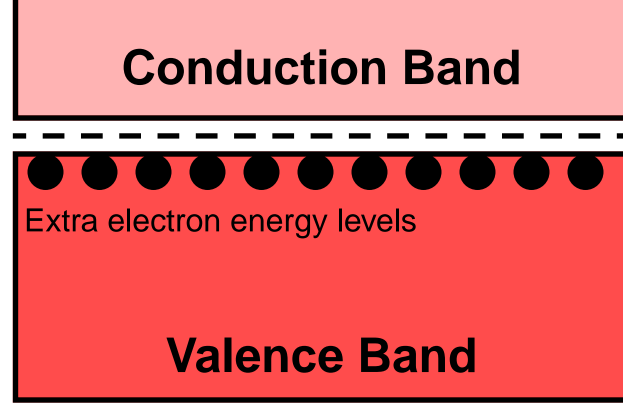
One Way to Think About It

Acceptor side



P-type

Donor side



N-type

- **P-type: Conduction band is pulled down close to the valence band by the creation of available holes (willing acceptors of free electrons)**
- **N-type: Valence band is pushed up close to the conduction band by the addition of mobile electrons**

Bruce Jacob

University of
Maryland
ECE Dept.

The P/N Junction

Acceptor side	Donor side
Conduction Band	Conduction Band
Extra hole energy levels	Extra electron energy levels
Valence Band	Valence Band
P-type	N-type

- **P-type: extra holes in band gap allow excitation of valence-band electrons, leaving mobile holes in valence band**
- **N-type: electron energy levels near the top of the band gap allow easy excitation of electrons into conduction band**

Bruce Jacob

University of
Maryland
ECE Dept.

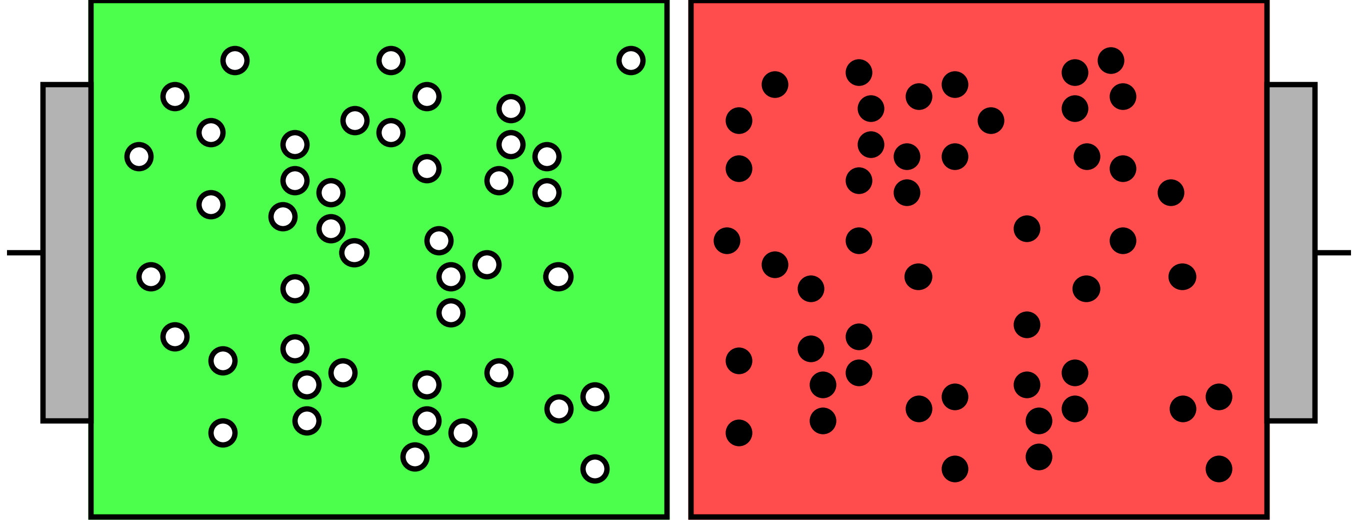
The P/N Junction

Bruce Jacob

University of
Maryland
ECE Dept.

The P/N Junction

DEPLETION REGION



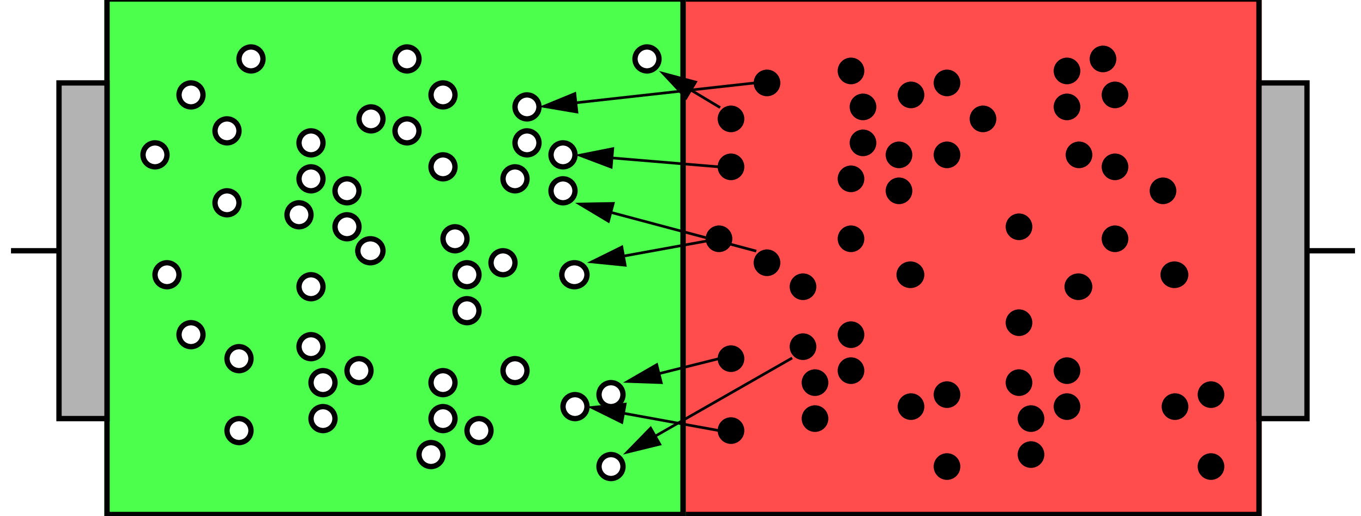
If not touching, nothing happens

Bruce Jacob

University of
Maryland
ECE Dept.

The P/N Junction

DEPLETION REGION



With a connection, electrons from n-region in conduction band diffuse across junction and combine with holes in p-region

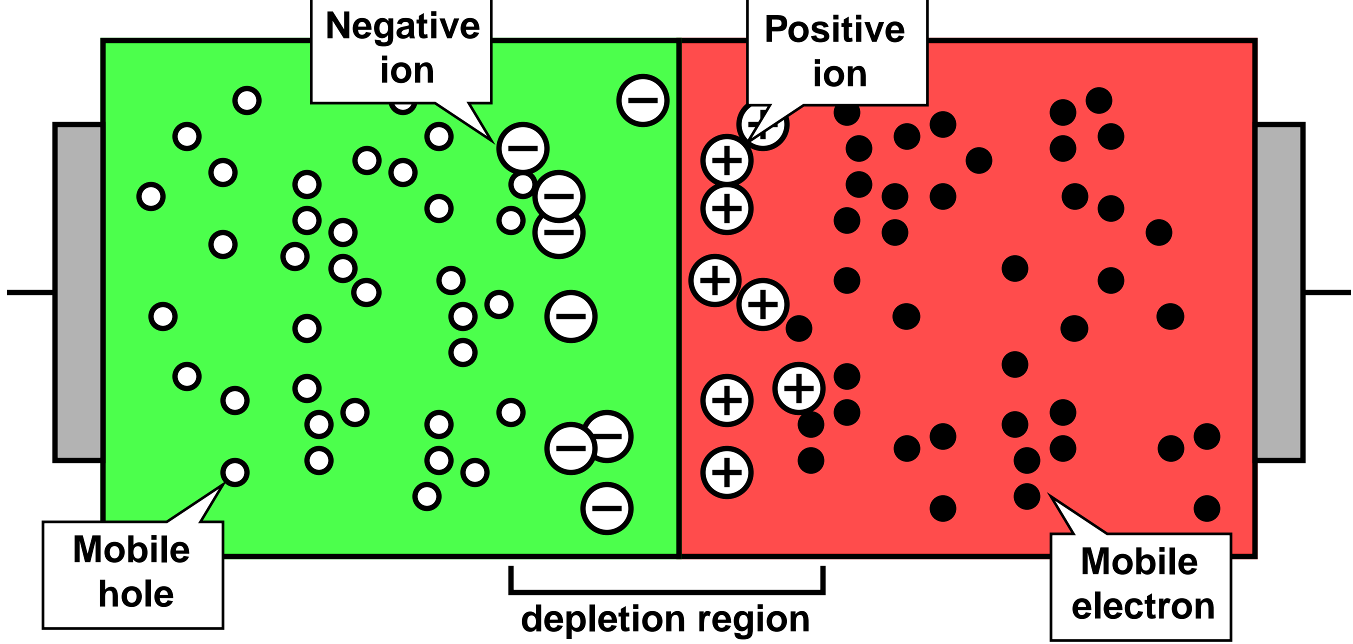
(why doesn't this continue indefinitely?)

Bruce Jacob

University of
Maryland
ECE Dept.

The P/N Junction

DEPLETION REGION



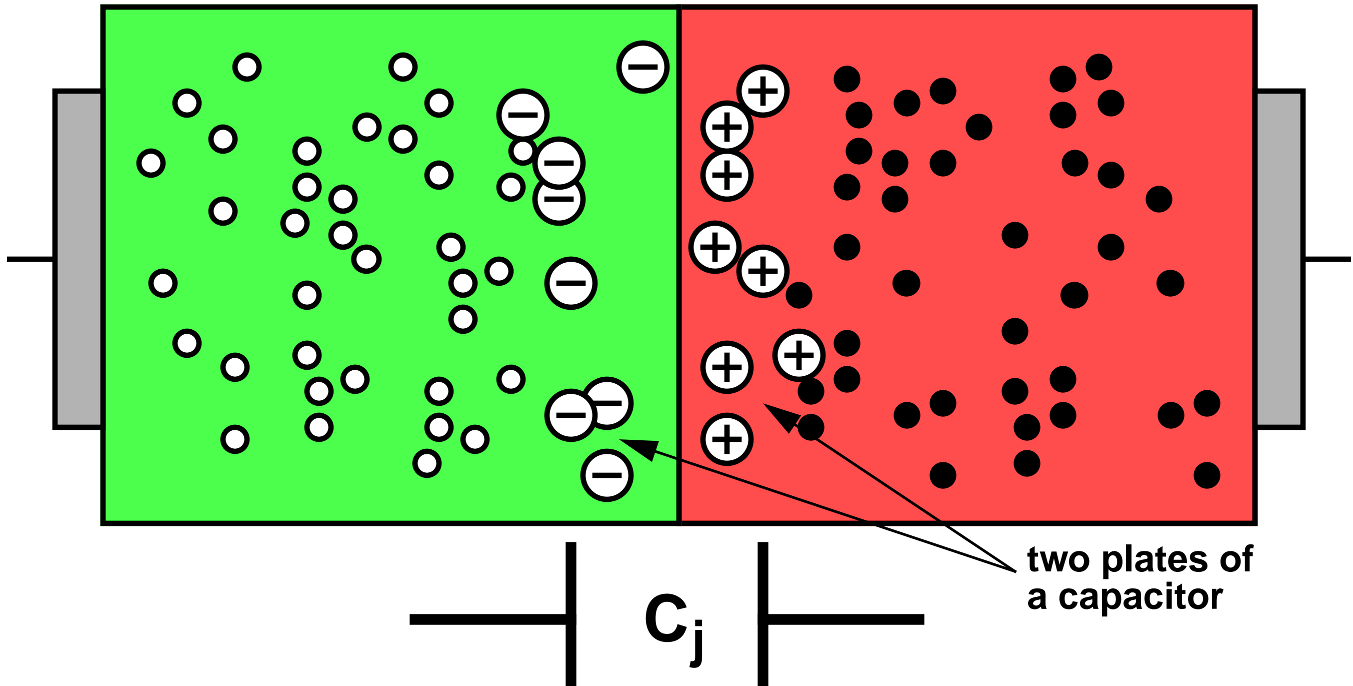
Ions are formed on both sides of junction (negative ion from filled hole; positive ion from removed electron). This forms a space charge that impedes further electron flow.

Bruce Jacob

University of
Maryland
ECE Dept.

The P/N Junction

DEPLETION REGION



Parasitic capacitance:

$$C_j = \frac{C_{j0}}{\left[1 - \frac{V_d}{\phi_0}\right]^m}$$

Built-in junction potential:

$$\phi_0 = \phi_T \cdot \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

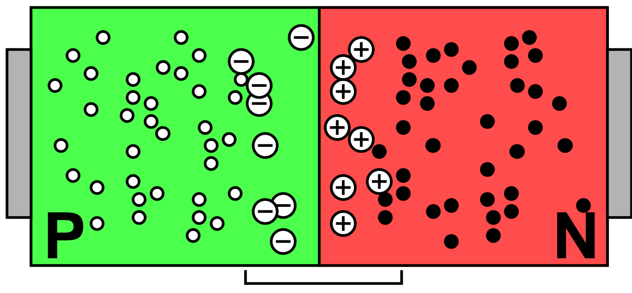
Bruce Jacob

University of
Maryland
ECE Dept.

The P/N Junction

BIAS EFFECT on DEPLETION REGION

Equilibrium



Conduction Band

Conduction Band

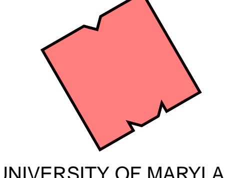
Extra hole energy levels

Valence Band

Extra electron energy levels

Valence Band

- **Upward = increased electron energy (must supply energy to make electron go up or hole to go down)**
- **Drift-diffusion equilibrium (current *is* flowing)**

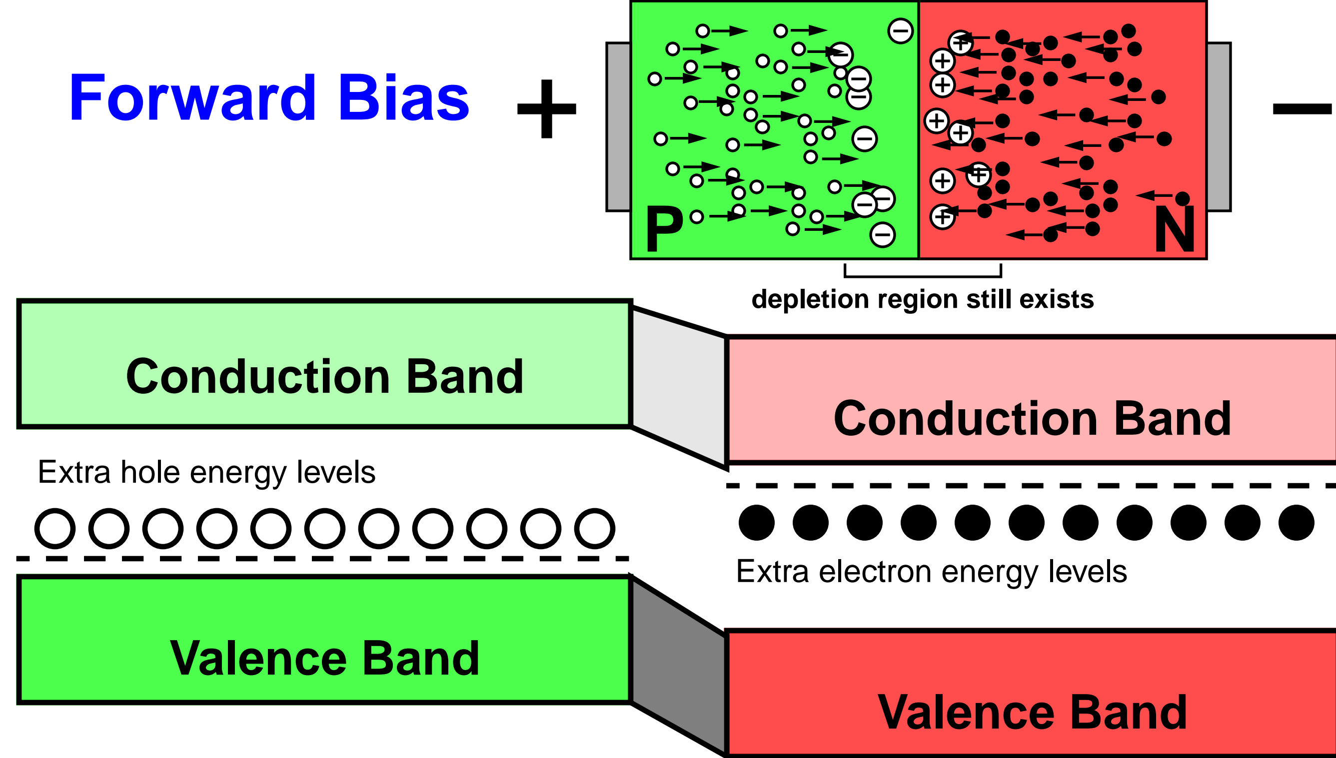


Bruce Jacob

University of
Maryland
ECE Dept.

The P/N Junction

BIAS EFFECT on DEPLETION REGION



P-side is made more positive relative to N-side, making it "downhill" to move an electron across the junction. Electron on N-side can fill a vacancy ("hole") on P-side & move from hole to hole to the left to positive terminal (hole "moves" right).

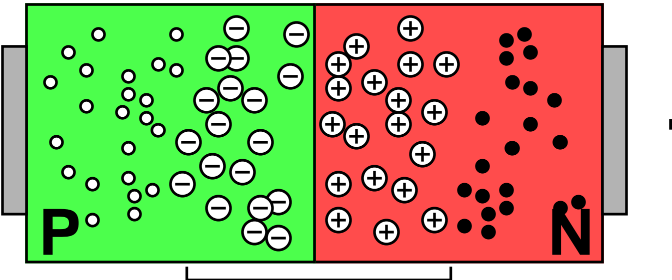
Bruce Jacob

University of
Maryland
ECE Dept.

The P/N Junction

BIAS EFFECT on DEPLETION REGION

Reverse Bias – +

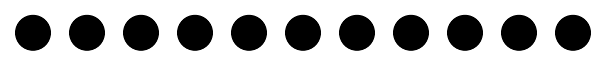


depletion region increases in size
until new potential = applied bias

Conduction Band

Extra hole energy levels

Valence Band

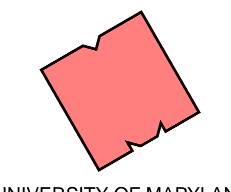


Conduction Band

Extra electron energy levels

Valence Band

P-side is made more negative relative to N-side, making it “uphill” to move an electron across the junction. Applied voltage impedes the flow of N-region electrons across the p/n junction. Initial transient electron flow is left to right; it stops when potential (widening depletion region) equals the applied voltage.

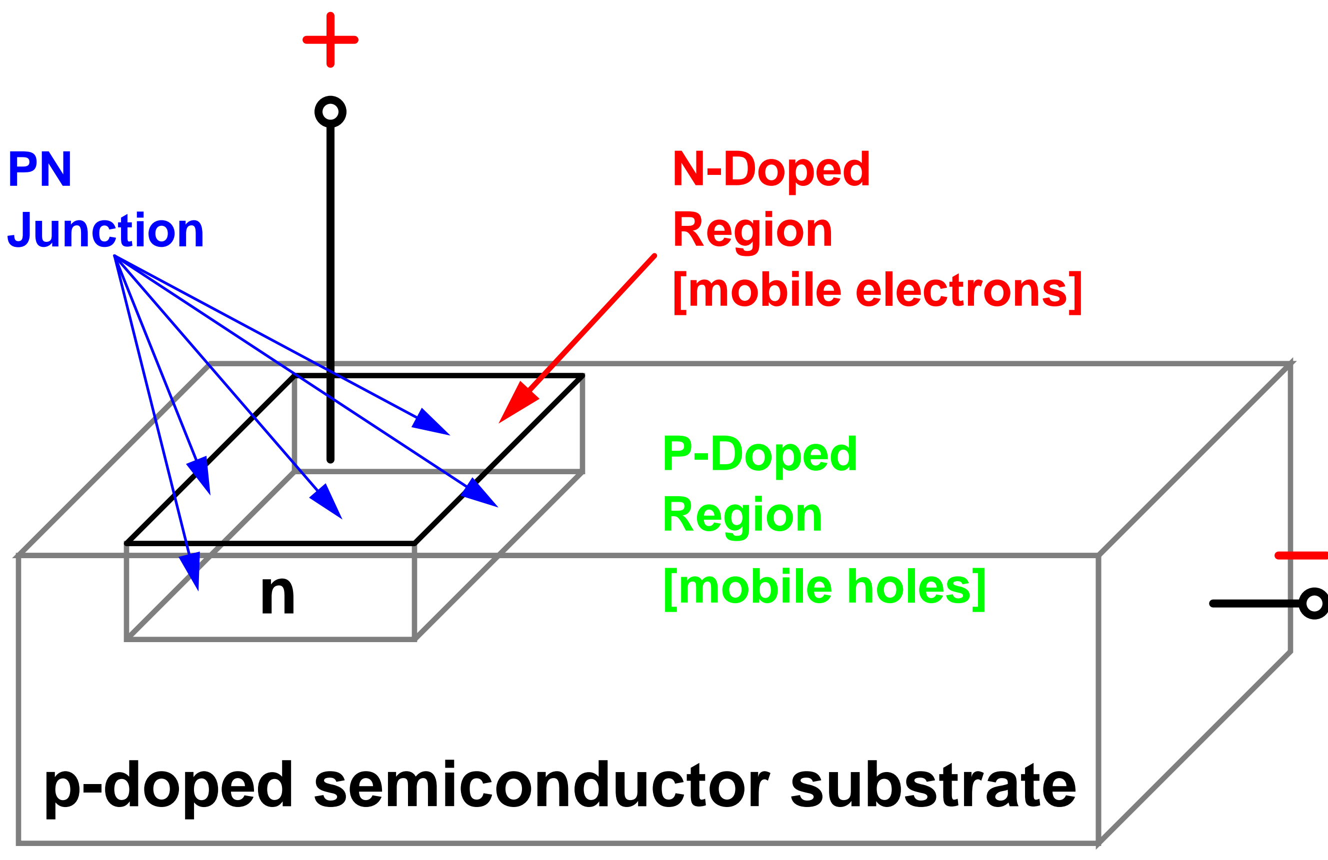


Bruce Jacob

University of
Maryland
ECE Dept.

MOS Transistors

MOS Transistor, reverse-biased:



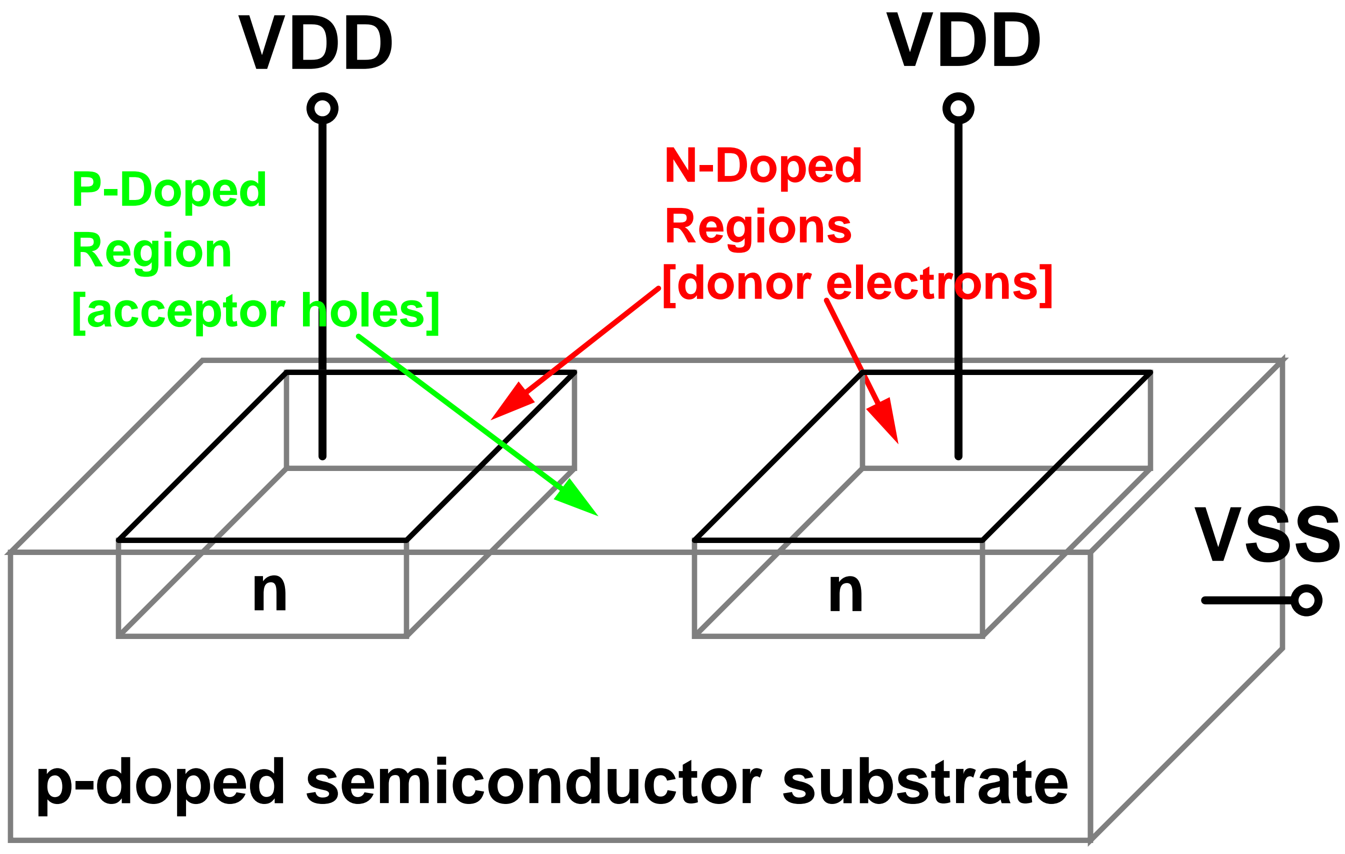
ENEE 359a
Lecture/s 3-5
Transistors &
CMOS Inverter

Bruce Jacob

University of
Maryland
ECE Dept.

MOS Transistors

MOS Transistor, reverse-biased:

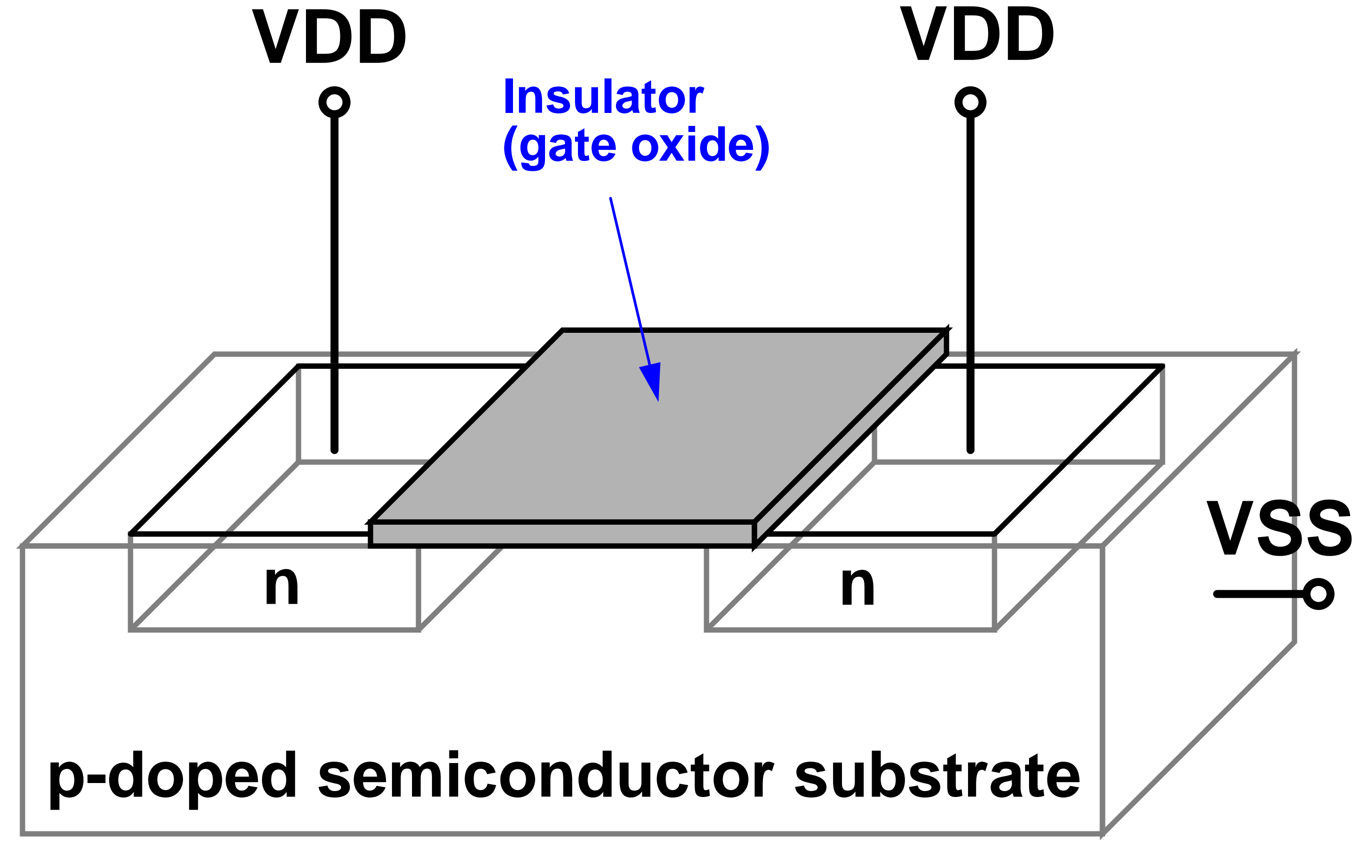


Bruce Jacob

University of
Maryland
ECE Dept.

MOS Transistors

MOS Transistor, reverse-biased:



Bruce Jacob

University of
Maryland
ECE Dept.

MOS Transistors

NMOS Transistor with gate:

Bruce Jacob

University of
Maryland
ECE Dept.

MOS Transistors

NMOS Transistor with bias voltages:

0

0

+

Conductor

Insulator
(gate oxide)

n

n

0

p-doped semiconductor substrate

Bruce Jacob

University of
Maryland
ECE Dept.

MOS Transistors

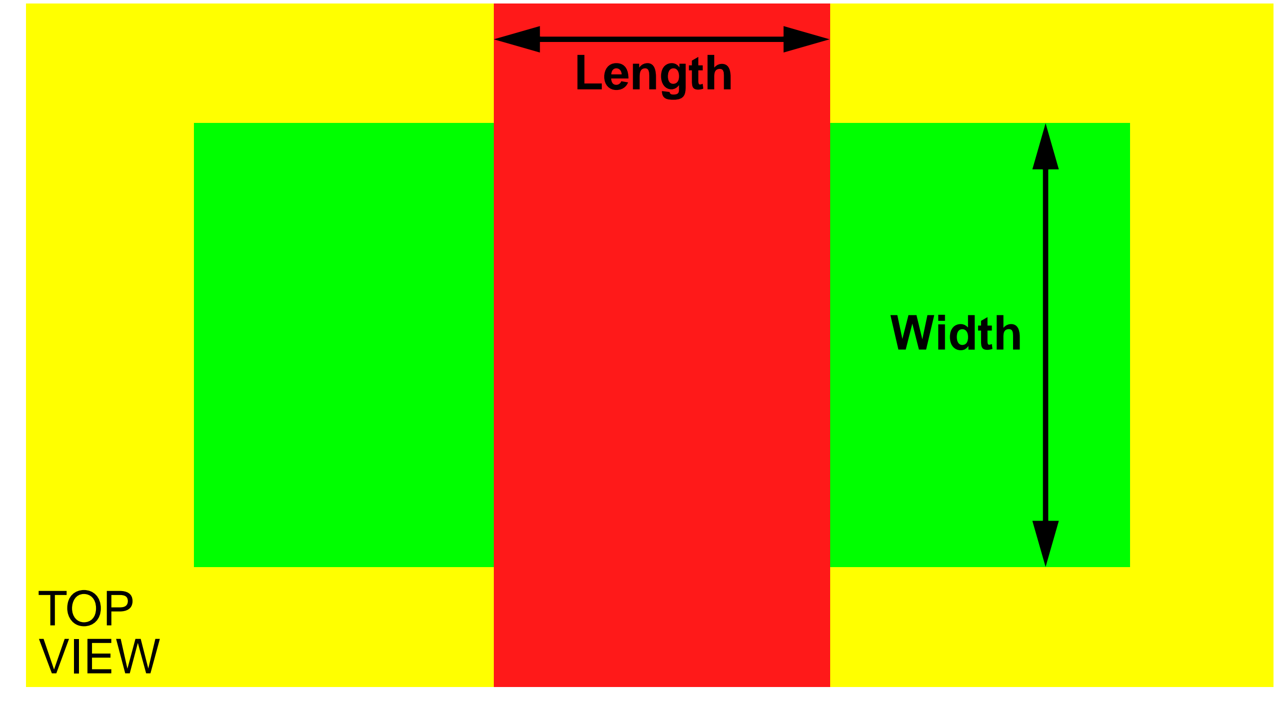
NMOS Transistor with bias voltages:

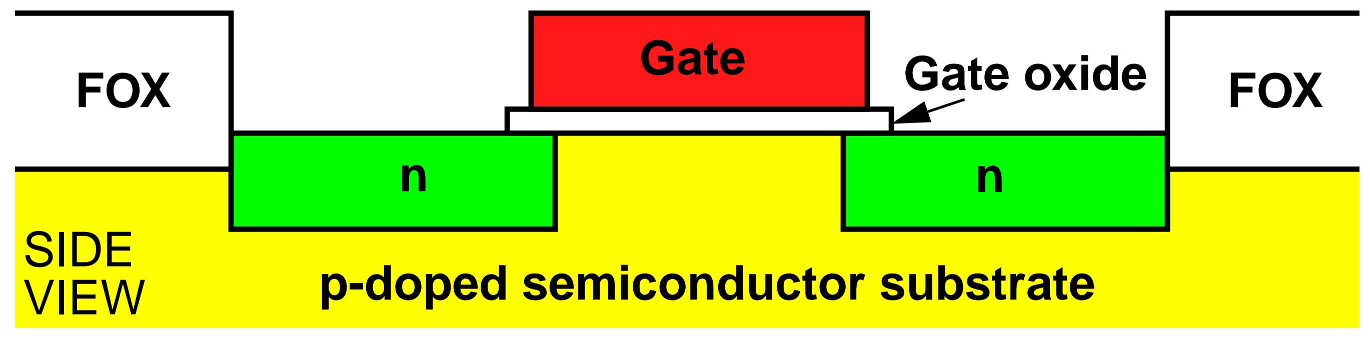
Bruce Jacob

University of
Maryland
ECE Dept.

MOS Transistors

NMOS Transistor, two views:





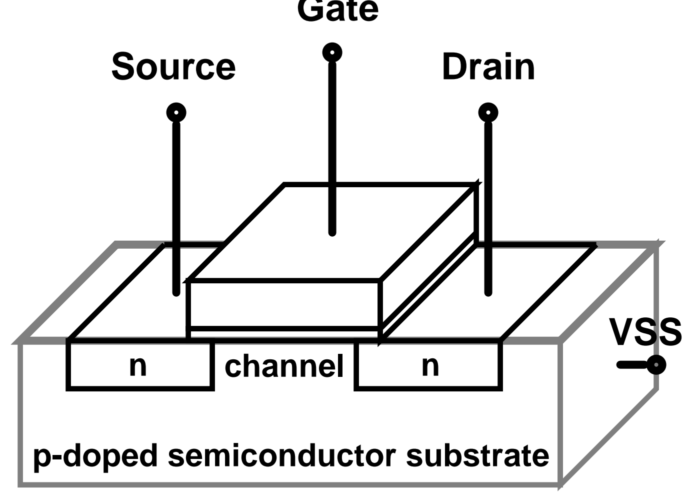
UNIVERSITY OF MARYLAND

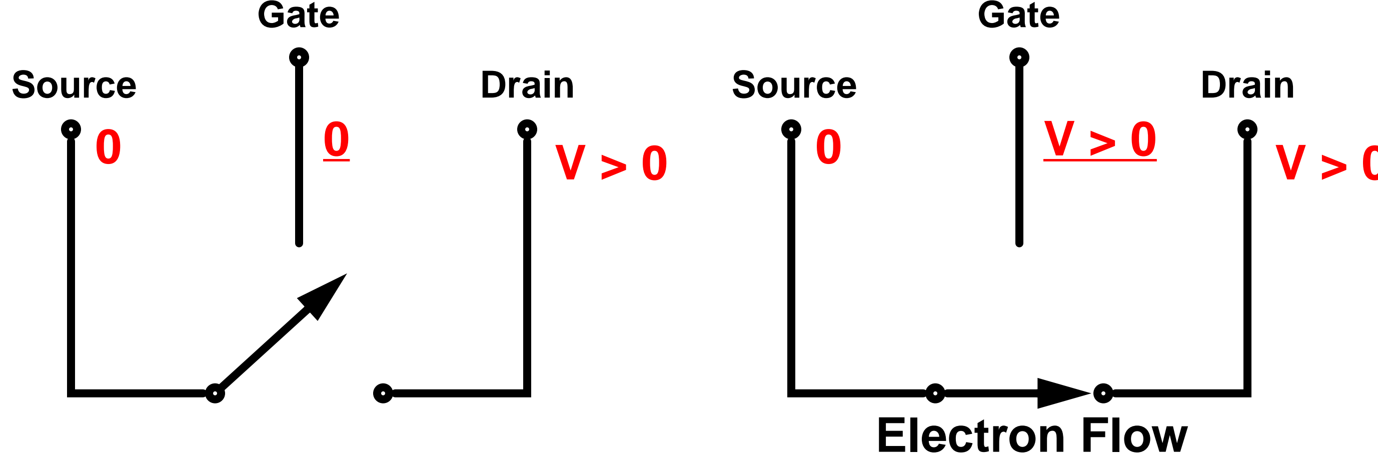
Bruce Jacob

University of
Maryland
ECE Dept.

MOS Transistors

NMOS Transistor with bias voltages:



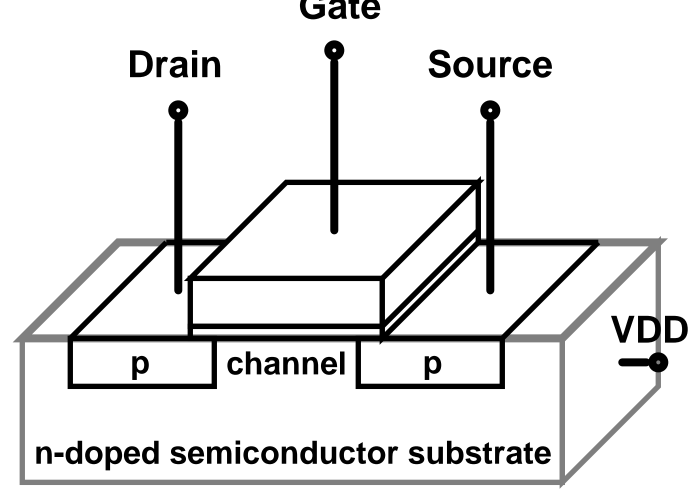


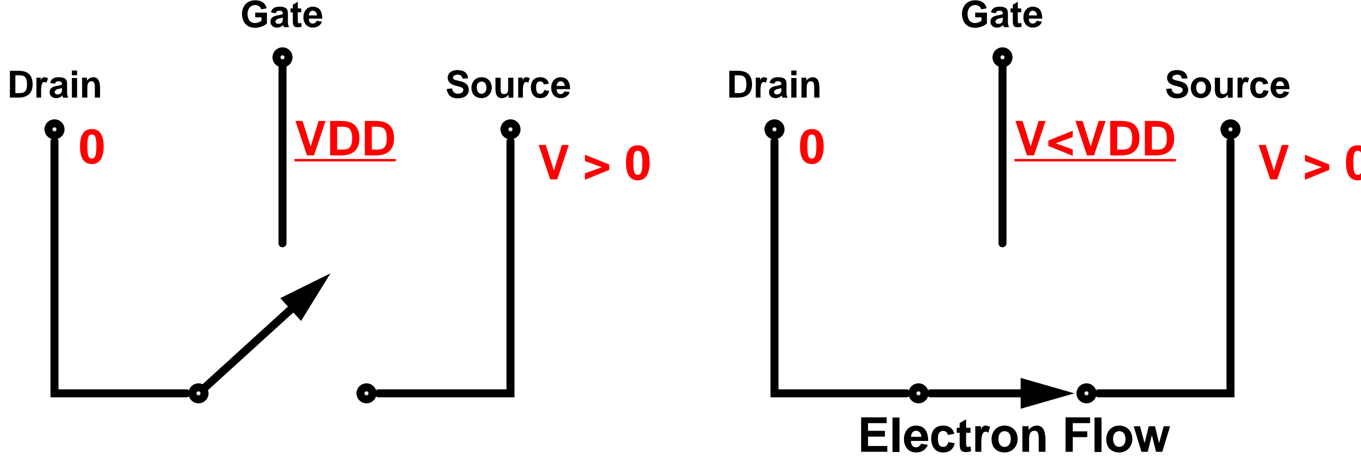
Bruce Jacob

University of
Maryland
ECE Dept.

MOS Transistors

PMOS Transistor with bias voltages:





Bruce Jacob

University of
Maryland
ECE Dept.

MOS Transistors

MOS Transistors:

Bruce Jacob

University of
Maryland
ECE Dept.

0.25 µm transistor (Bell Labs)

Silicide

Poly

Gate oxide

Source & Drain

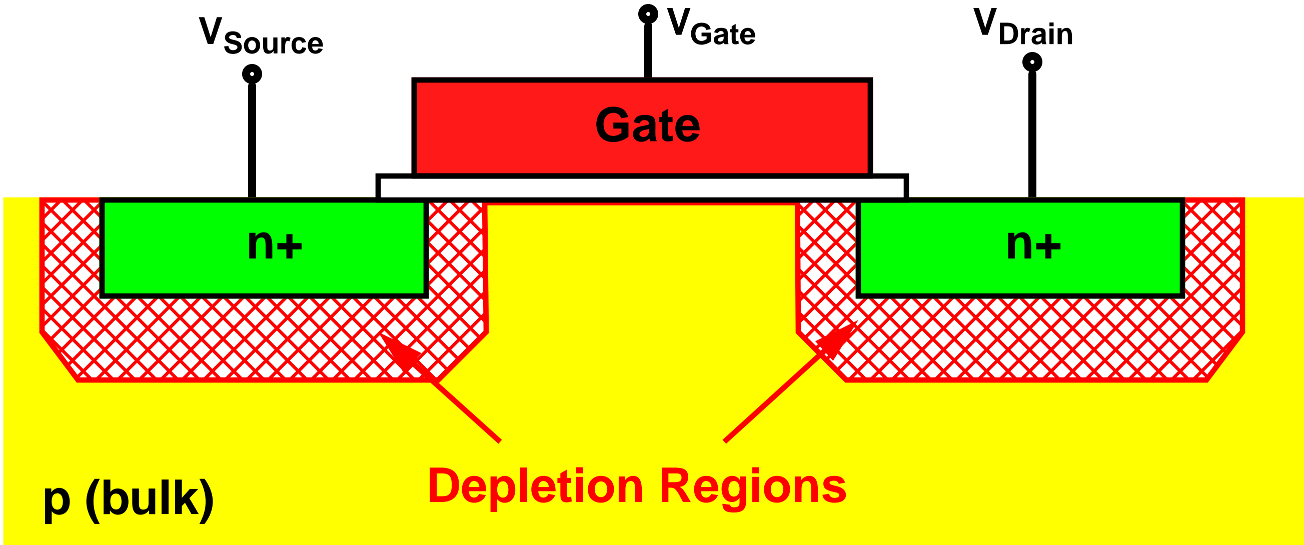
Poly+silicide = “polycide gate” (lower R)

ENEE 359a
Lecture/s 3-5
Transistors &
CMOS Inverter

Bruce Jacob

University of
Maryland
ECE Dept.

MOS Behavior



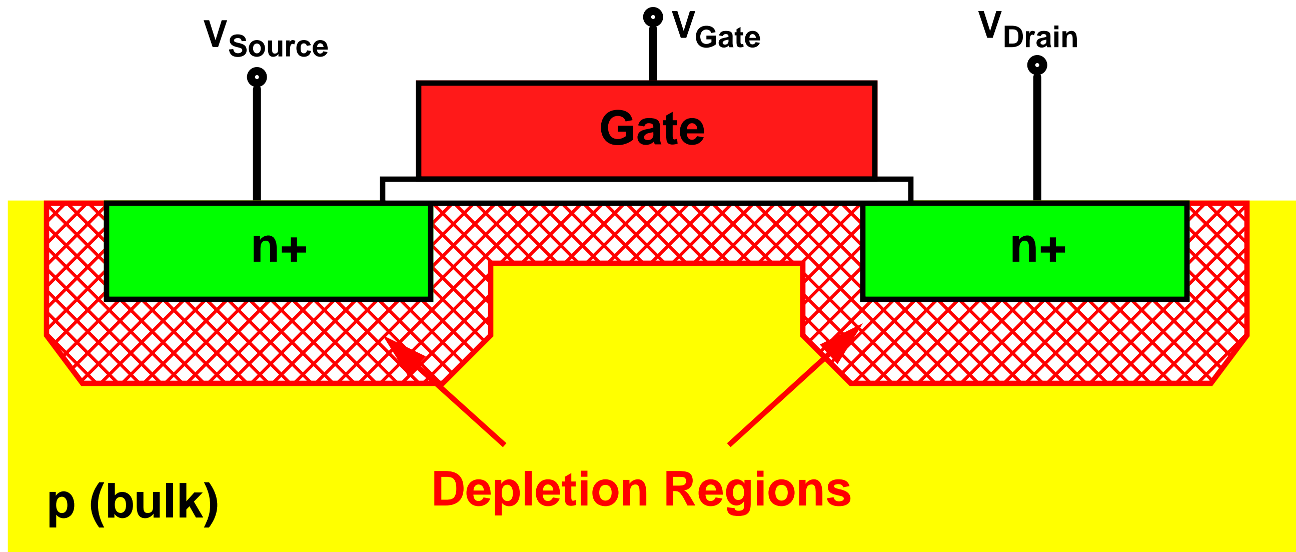
UNIVERSITY OF MARYLAND

ENEE 359a
Lecture/s 3-5
Transistors &
CMOS Inverter

Bruce Jacob

University of
Maryland
ECE Dept.

MOS Behavior



$V_S = 0V$ $V_G = 0.5V$ $V_D = 0V$

Charge Density

Gate

Oxide

Substrate
(p-type)

Depletion layer

x (depth)

Bruce Jacob

University of
Maryland
ECE Dept.

MOS Behavior

V_{Source}

Channel

V_{Gate}

Free electrons

V_{Drain}

Gate

n+

n+

Depletion Regions

Inversion Layer forms when $V_{GS} > V_T$

Assume $V_T = 0.75V$ (threshold voltage)

p (bulk)

$V_S = 0V$ $V_G = 1V$ $V_D = 0V$

Charge Density

Gate

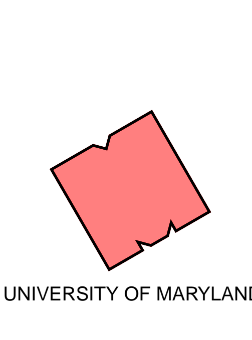
Oxide

Inversion layer

Substrate (p-type)

Depletion layer

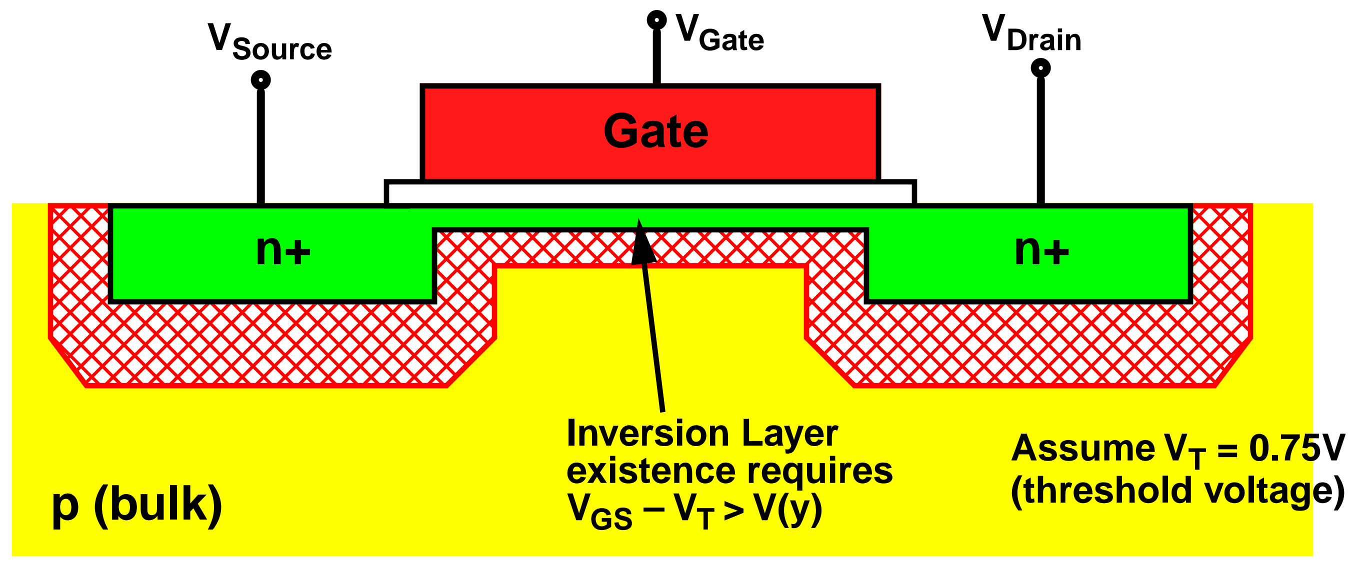
x (depth)



Bruce Jacob

University of
Maryland
ECE Dept.

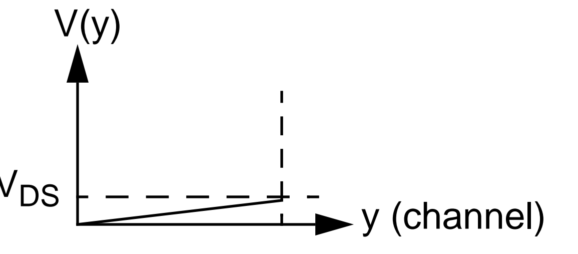
MOS Behavior: linear region

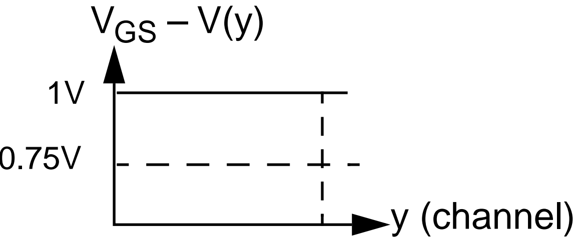


$V_S = 0V$ $V_G = 1V$ $V_D = 0.001V$

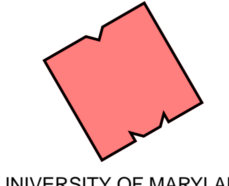
dielectric constant, electron mobility, oxide thickness

$$I_{DS} = \mu_n \frac{\varepsilon_{ox}}{t_{ox}} \left(\frac{W}{L}\right)(V_{GS} - V_T)V_{DS}$$





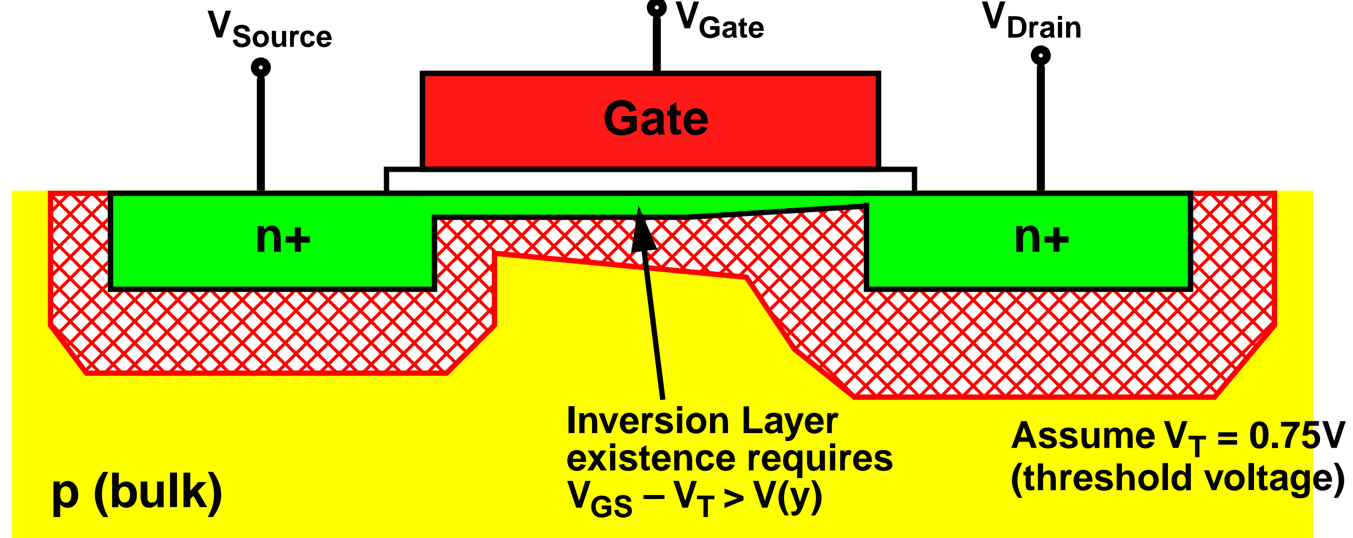
True when $V_{GS} > V_T$ & $V_{DS} \ll V_{GS} - V_T$



Bruce Jacob

University of
Maryland
ECE Dept.

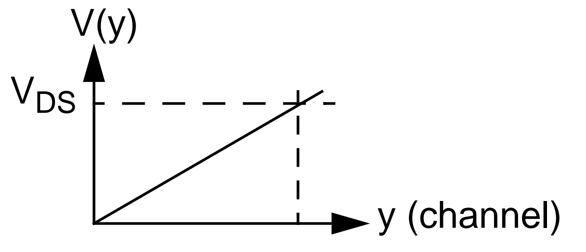
MOS Behavior: ‘linear’ region

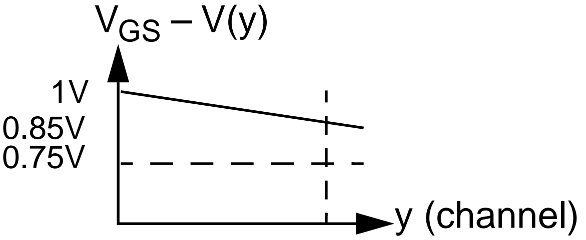


$V_S = 0V$ $\quad V_G = 1V$ $\quad V_D = 0.15V$

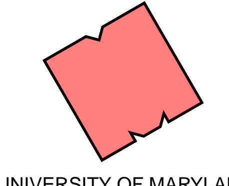
$$I_{DS} = \mu_n \frac{\varepsilon_{ox}}{t_{ox}} \left(\frac{W}{L}\right) \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

electron mobility; dielectric constant; oxide thickness





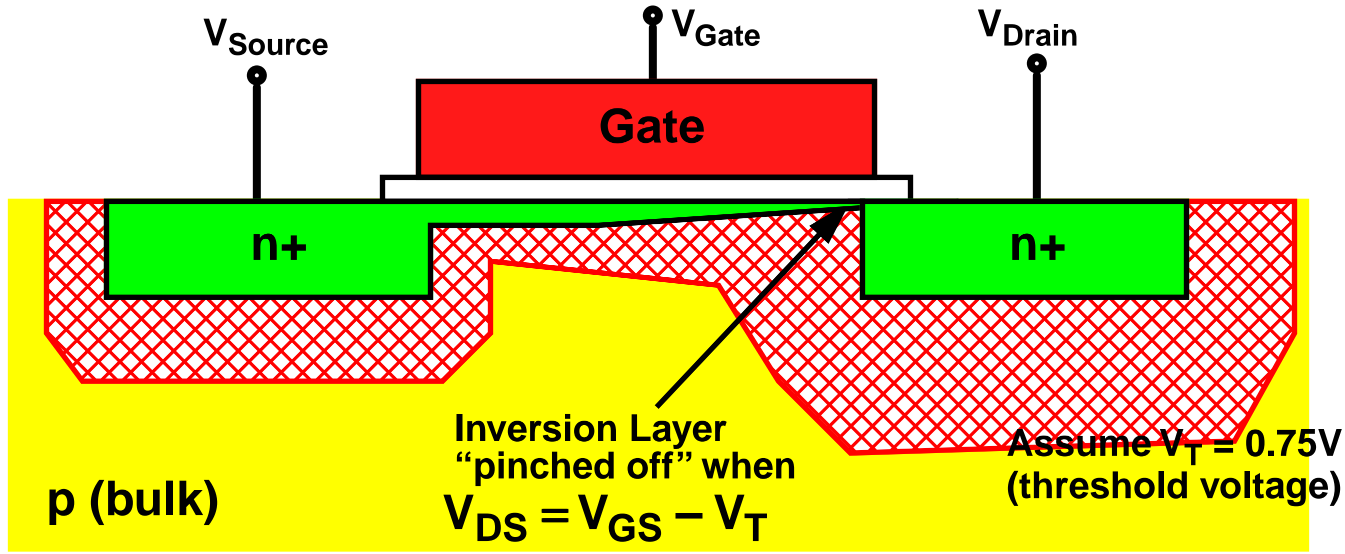
True when $V_{GS} > V_T$ & $V_{DS} \leq V_{GS} - V_T$



Bruce Jacob

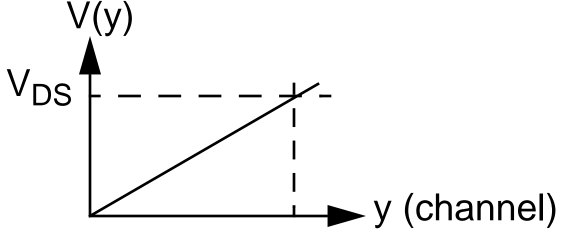
University of
Maryland
ECE Dept.

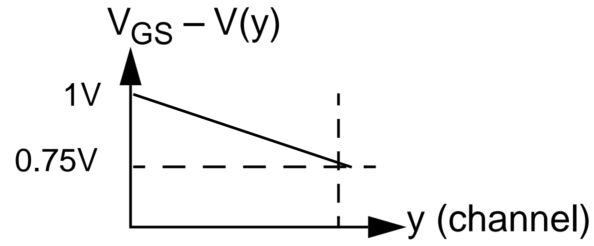
MOS Behavior: saturation



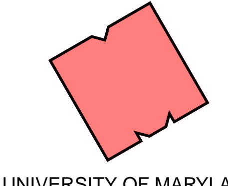
$V_S = 0V$ $V_G = 1V$ $V_D = 0.25V$

$$I_{DS} = \frac{1}{2}\left(\mu_n \frac{\varepsilon_{ox}}{t_{ox}}\left(\frac{W}{L}\right)\right)(V_{GS} - V_T)^2$$





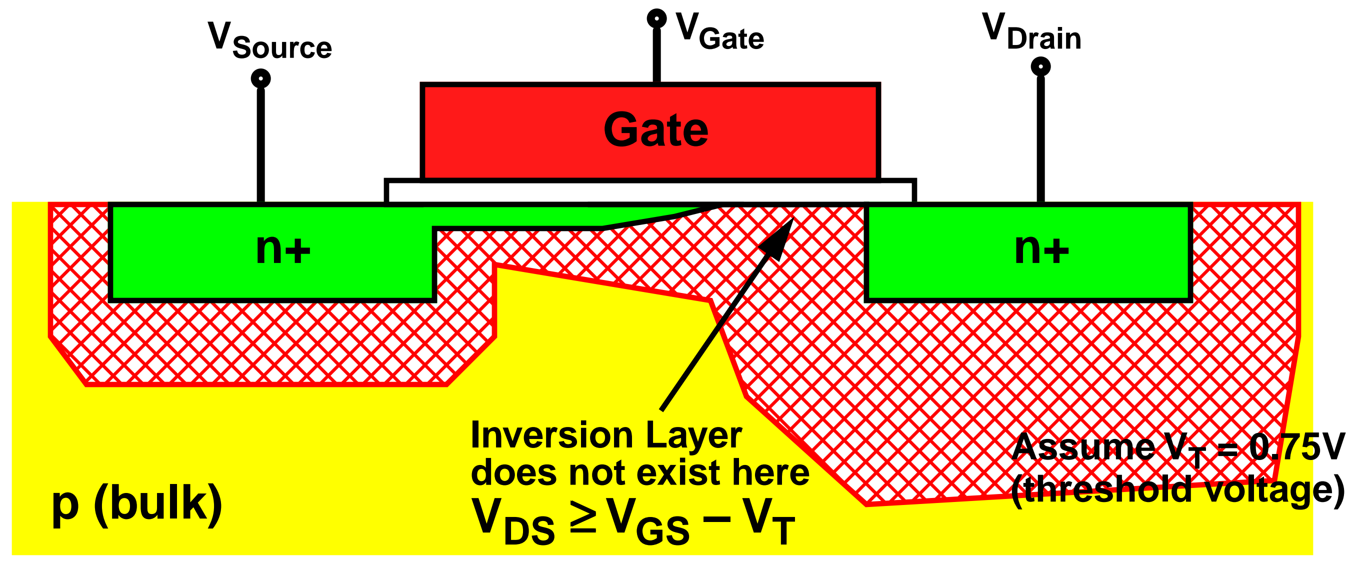
True when $V_{GS} > V_T$ & $V_{DS} = V_{GS} - V_T$



Bruce Jacob

University of
Maryland
ECE Dept.

MOS Behavior: modulation



$V_S = 0V$ $V_G = 1V$ $V_D = 0.35V$

$$I_{DS} = \frac{1}{2}\left(\mu_n \frac{\varepsilon_{ox}}{t_{ox}}\left(\frac{W}{L}\right)\right)(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

effective channel length decreases

length modulation factor

V(y)

V_{DS}

y (channel)

$V_{GS} - V(y)$

1V

0.75V

0.65V

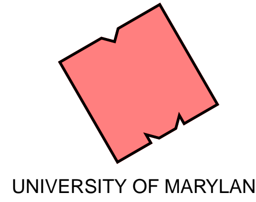
y (channel)

over this range, effective gate potential is not sufficient to create inversion layer

True when $V_{GS} > V_T$ & $V_{DS} \geq V_{GS} - V_T$

Bruce Jacob

University of
Maryland
ECE Dept.



UNIVERSITY OF MARYLAND

Example of Drain Current

Values for generic 0.5 µm process:

	k' (transconductance) $= \mu_n \frac{\varepsilon_{ox}}{t_{ox}}$	$\mathbf{V_T}$
n-type	$k'_n = 73\ \mu A/V^2$	0.7V
p-type	$k'_p = 21\ \mu A/V^2$	-0.8V

Assume W/L = 3/2, V_{GS} = 2V, find I_{DS} for NMOS device at saturation point:

$$I_{DS} = \frac{1}{2}\left(k'\frac{W}{L}\right)(V_{GS} - V_T)^2$$

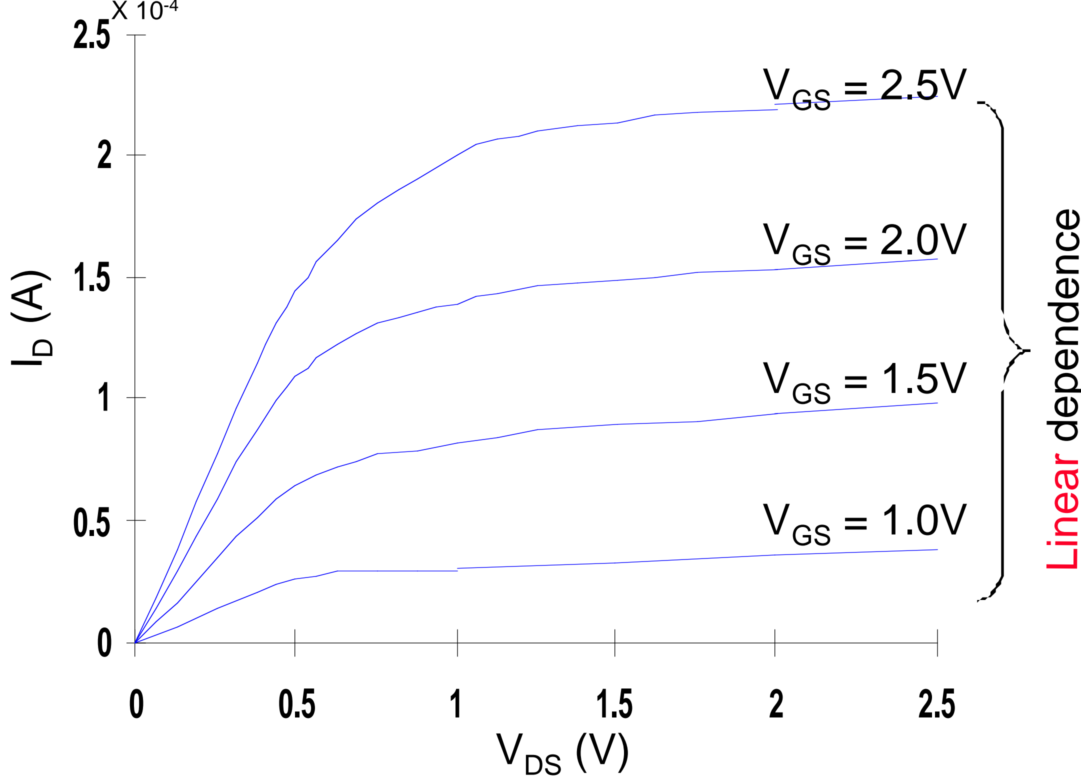
$$I_{DS} = \frac{1}{2}\left(73\frac{\mu A}{V^2}\right)\left(\frac{3}{2}\right)(2V - 0.7V)^2 = 93\mu A$$

ENEE 359a
Lecture/s 3-5
Transistors &
CMOS Inverter

Bruce Jacob

University of
Maryland
ECE Dept.

NMOS I-V Plot



NMOS transistor, 0.25um, L_d = 0.25um, W/L = 1.5, V_{DD} = 2.5V, V_T = 0.4V

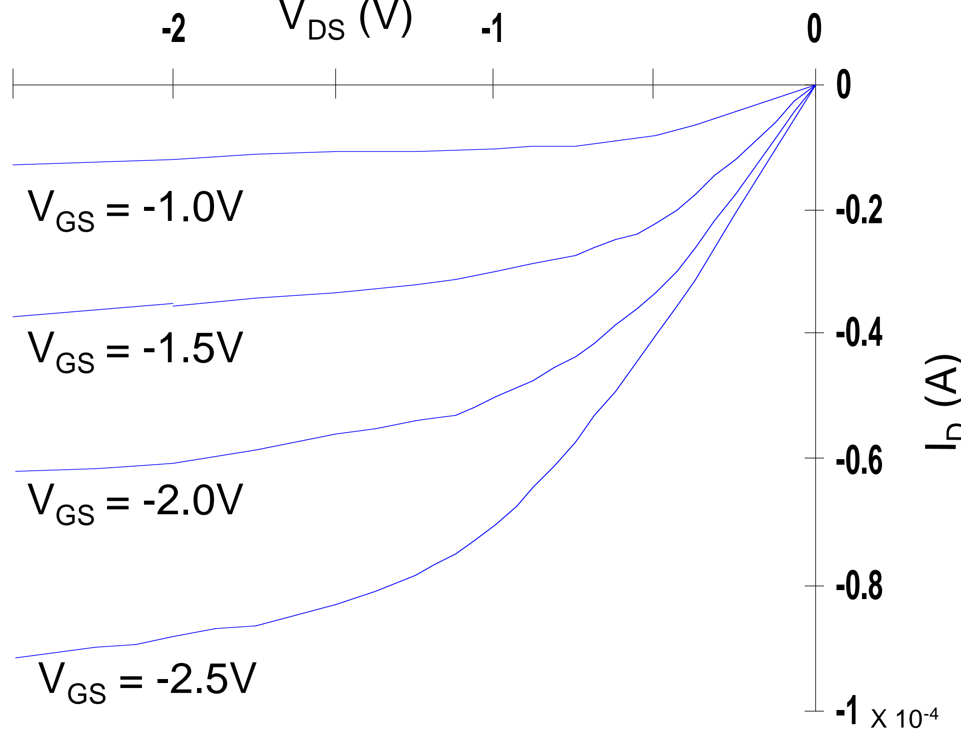
UNIVERSITY OF MARYLAND

Bruce Jacob

University of
Maryland
ECE Dept.

PMOS I-V Plot

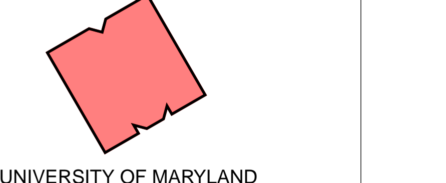
- All polarities of all voltages and currents are reversed



PMOS transistor, 0.25um, L_d = 0.25um, W/L = 1.5, V_{DD} = 2.5V, V_T = -0.4V

Note y-axis scale (because $W/L_p = W/L_n$)

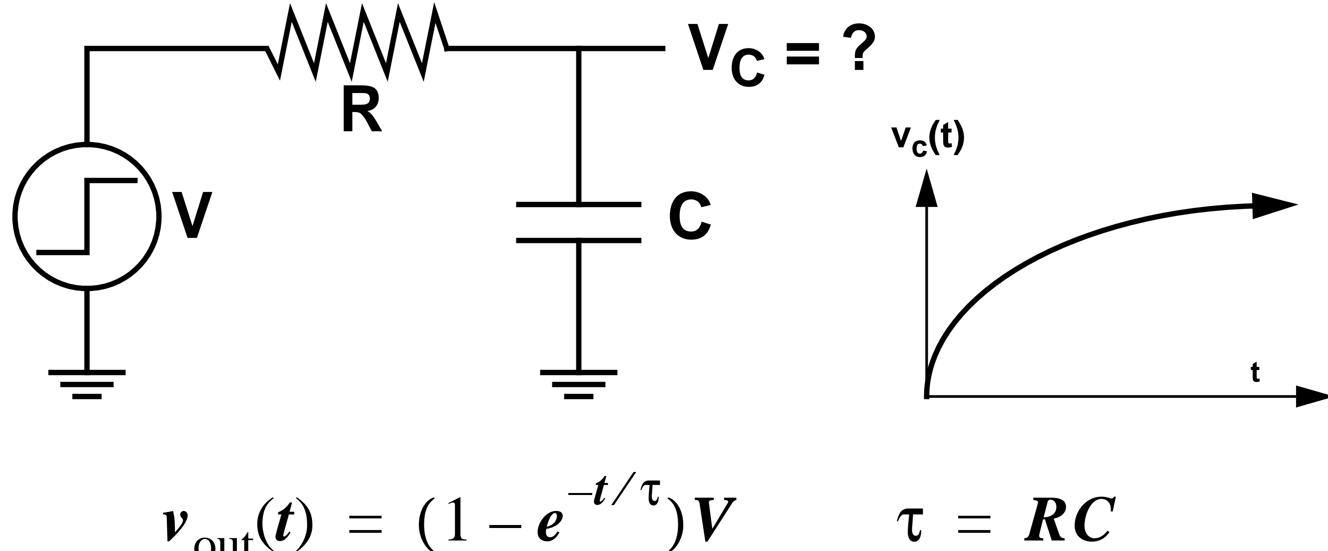
(*drive current:* I_D when $V_{GS} = V_{DS} = V_{DD}$)



Bruce Jacob

University of
Maryland
ECE Dept.

Review: RC Circuits



$$v_{out}(t) = (1 - e^{-t/\tau})V \qquad \tau = RC$$

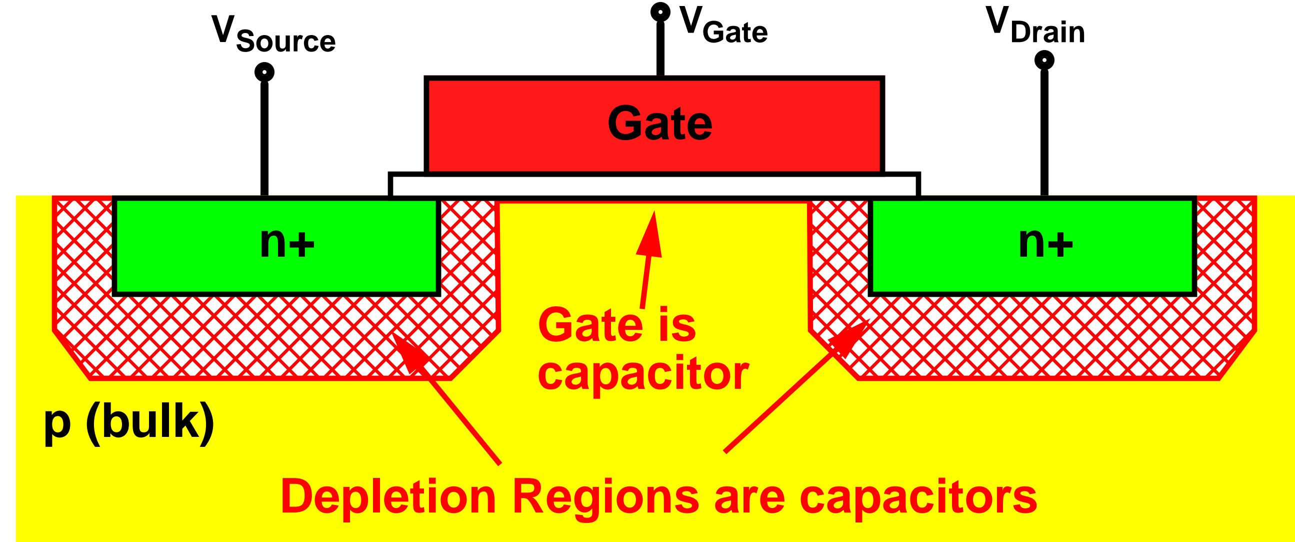
RC time-constant: dictates how rapidly the output voltage reacts to the voltage rise on input (step function).

Larger RC, slower response

Bruce Jacob

University of
Maryland
ECE Dept.

Capacitances



$$C_{gate} = \frac{WL\varepsilon_{ox}}{t_{ox}} \qquad C_{SC} = \frac{A\varepsilon_{si}}{t_{si}} \qquad C_{diff} = \frac{I \cdot \tau_c}{V_{th}}$$

Yes, there are others …

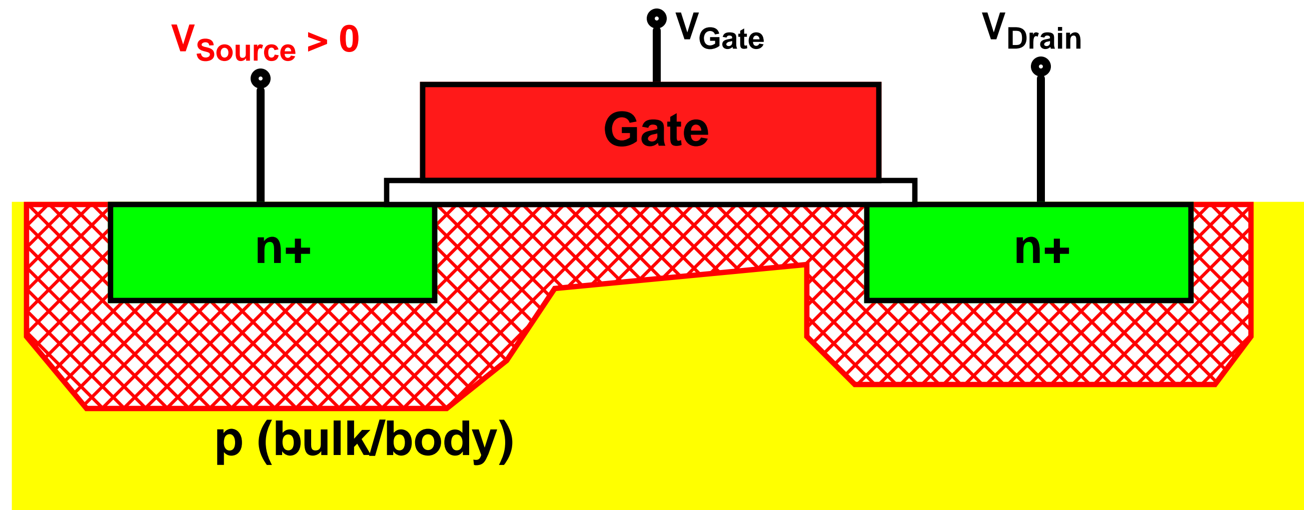
Result: parasitic capacitances hinder switching speeds

ENEE 359a
Lecture/s 3-5
Transistors &
CMOS Inverter

Bruce Jacob

University of
Maryland
ECE Dept.

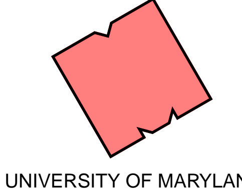
Body Effect



- Suppose source and body are not in equilibrium: reverse bias increases size of depletion region around that diode (and changes its parasitic capacitance)
- Called “body effect” … it changes the threshold voltage for that device

$$\Delta V_t = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}\left(\sqrt{\phi_S + V_{SB}} - \sqrt{\phi_S}\right)$$

But can it happen?



UNIVERSITY OF MARYLAND

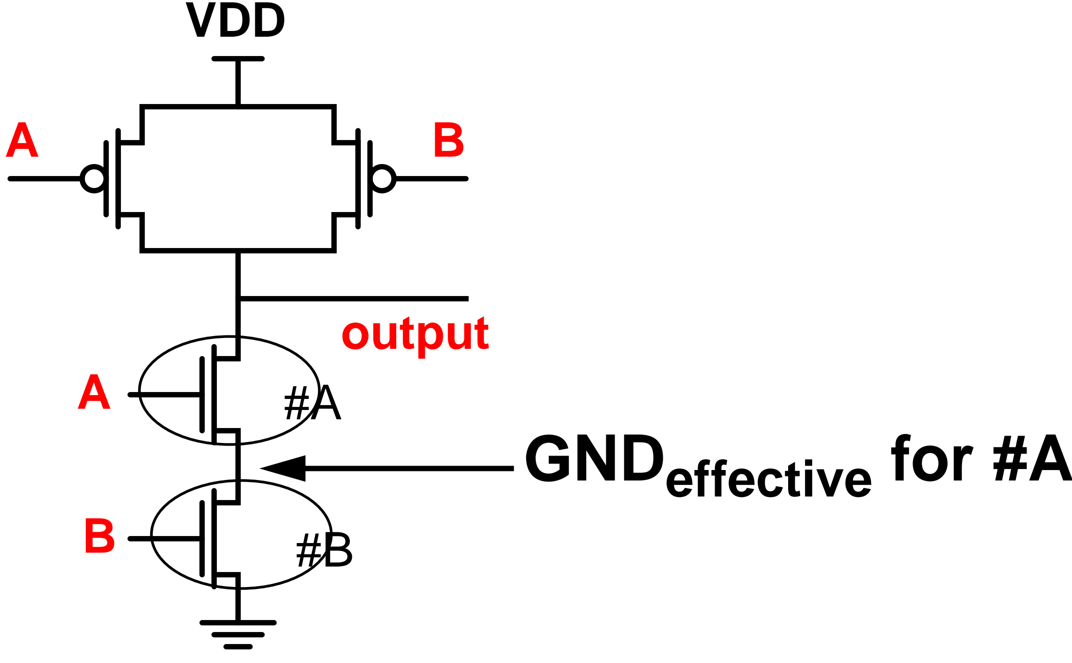
ENEE 359a
Lecture/s 3-5
Transistors &
CMOS Inverter

Bruce Jacob

University of
Maryland
ECE Dept.

Body Effect

NAND gate



- If #B propagates signal in non-zero time, the effective source voltage for #A can go positive (higher than ground)
- Perspective: Things start to get interesting when you start connecting these things together …

UNIVERSITY OF MARYLAND

ENEE 359a
Lecture/s 3-5
Transistors &
CMOS Inverter

Bruce Jacob

University of
Maryland
ECE Dept.

CMOS Inverter Layout I

N-regions for source, drain

Gate (poly)

P-regions and gate for PMOS device

input

GND

NMOS

output

PMOS

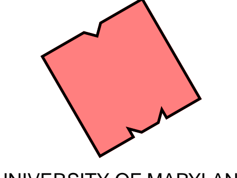
VDD

N-Well

Cut line

Bruce Jacob

University of
Maryland
ECE Dept.



CMOS Inverter Layout II

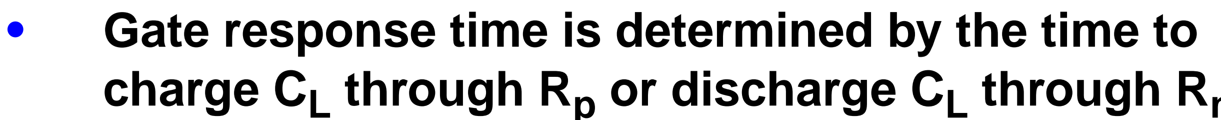
Another view (note: wells/tubs not shown)

ENEE 359a
Lecture/s 3-5
Transistors &
CMOS Inverter

Bruce Jacob

University of
Maryland
ECE Dept.

CMOS Inverter: Analysis



- Gate response time is determined by the time to charge C_L through R_p or discharge C_L through R_n

Bruce Jacob

University of
Maryland
ECE Dept.

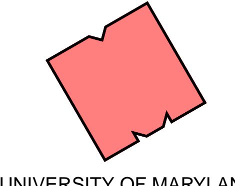
CMOS Inverter: Transfer Plot

ENEE 359a
Lecture/s 3-5
Transistors &
CMOS Inverter

Bruce Jacob

University of
Maryland
ECE Dept.

SLIDE 52



CMOS Inverter: Current

Bruce Jacob

University of
Maryland
ECE Dept.

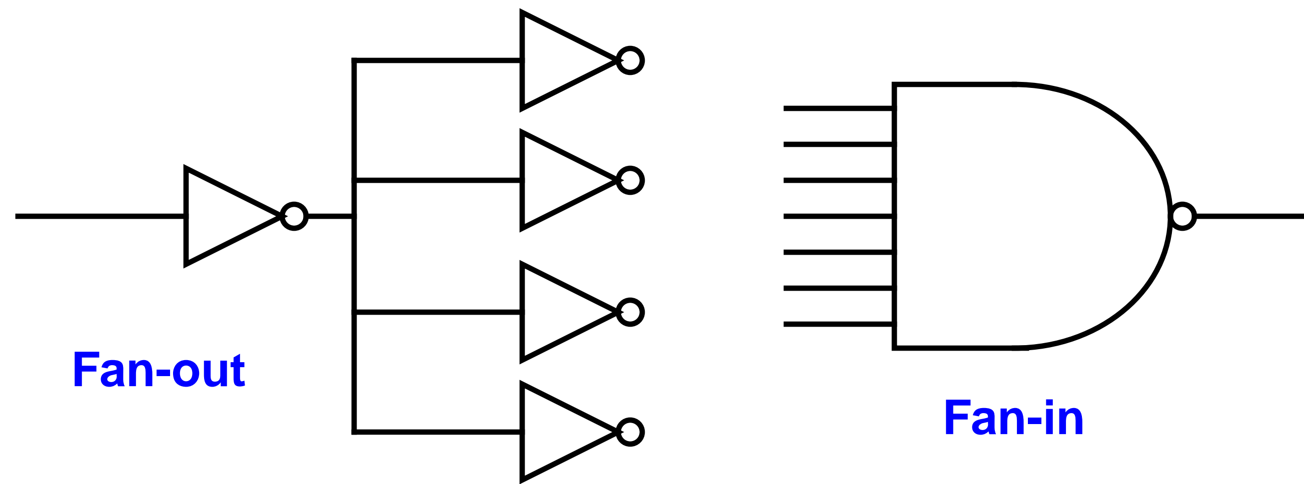
Properties of CMOS

- **Full rail-to-rail swing -> high noise margins**
- **Logic levels not dependent upon the relative device sizes -> transistors can be minimum size -> ratioless**
- **Always a path to Vdd or GND in steady state -> low output impedance (output resistance in kΩ range) -> large fan-out (albeit with degraded performance)**
- **Extremely high input resistance (gate of MOS transistor is near perfect insulator) -> nearly zero steady-state input current**
- **No direct path steady-state between power and ground -> no static power dissipation**
- **Propagation delay function of load capacitance and resistance of transistors**

Bruce Jacob

University of
Maryland
ECE Dept.

Capacitive Load, etc.



Fan-out: number of gates connected to the output of the driving date

- **Gates with large fan-out are slower**

Fan-in: the number of inuts to the gate

- **Gates with large fan-in are bigger and slower**

ENEE 359a
Lecture/s 3-5
Transistors &
CMOS Inverter

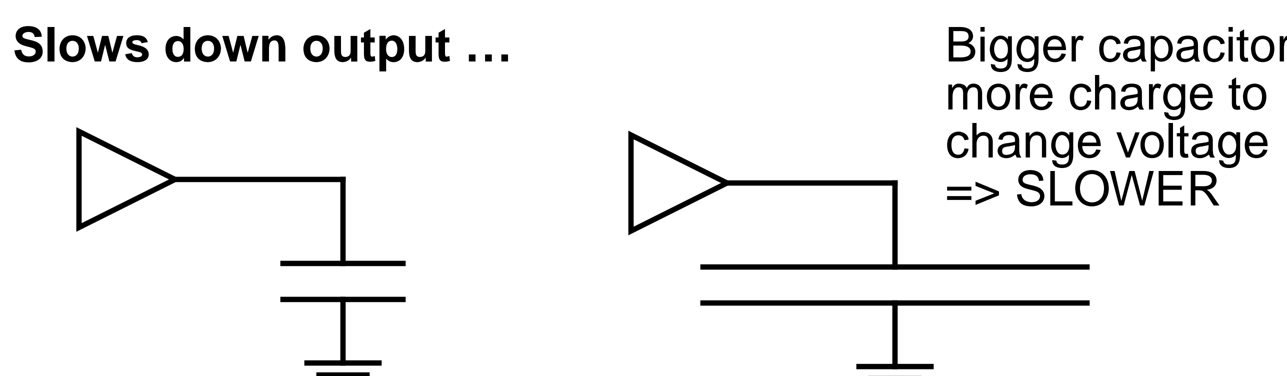
Bruce Jacob

University of
Maryland
ECE Dept.

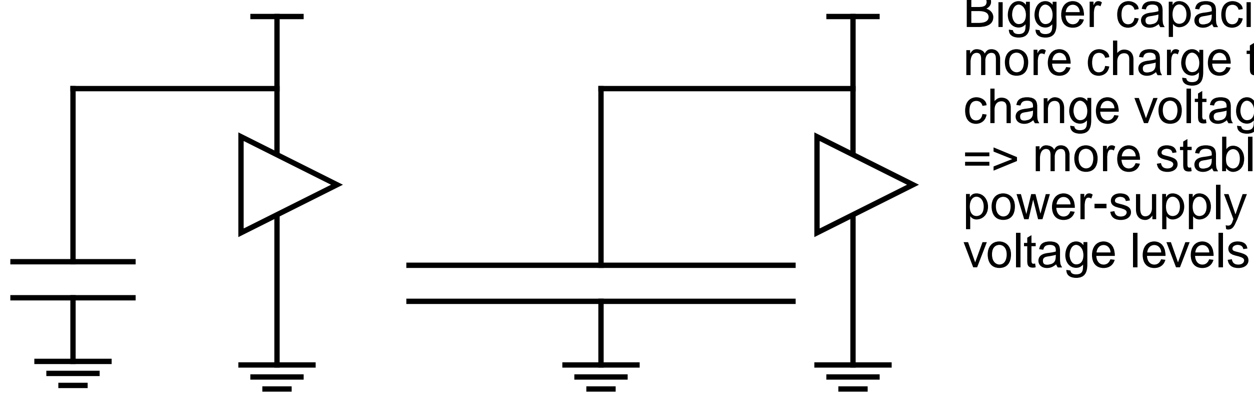
Aside:is capacitance all bad?

Slows down output …

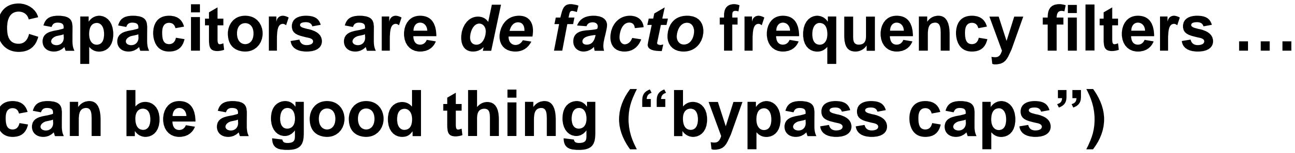
Bigger capacitor, more charge to change voltage => SLOWER



… but stabilizes power supply



Bigger capacitor, more charge to change voltage => more stable power-supply voltage levels



Capacitors are *de facto* frequency filters …

can be a good thing (“bypass caps”)

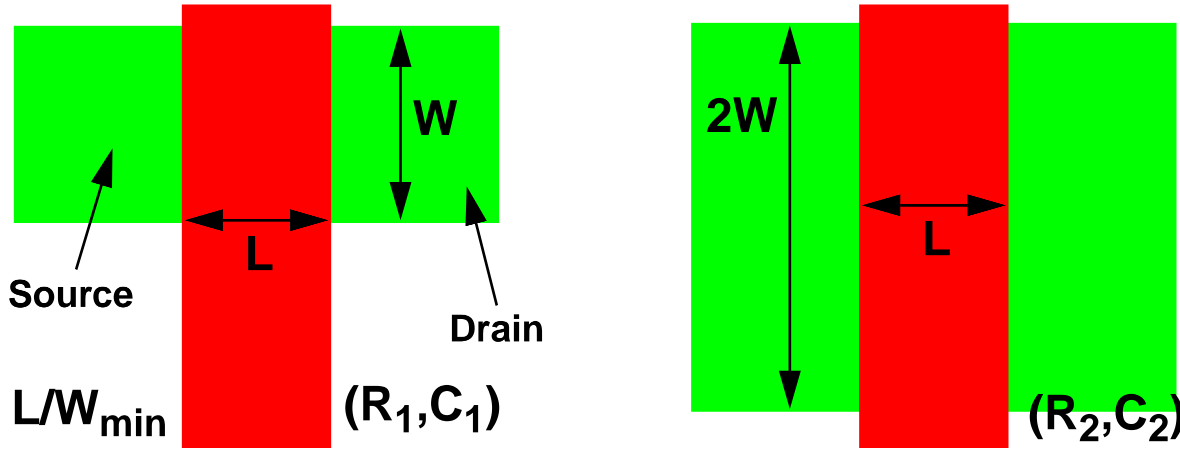
UNIVERSITY OF MARYLAND

ENEE 359a
Lecture/s 3-5
Transistors &
CMOS Inverter

Bruce Jacob

University of
Maryland
ECE Dept.

Transistor Sizing I

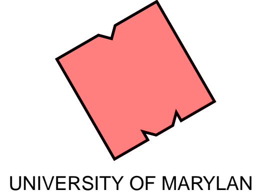


The electrical characteristics of transistors determine the switching speed of a circuit

- Need to select the aspect ratios $(W/L)_n$ and $(W/L)_p$ of *every* FET in the circuit

Define *Unit Transistor* (R_1, C_1)

- L/W_{min}-> highest resistance
- $R_2 = R_1 \div 2$ and $C_2 = 2 \bullet C_1$
- Separate nFET and pFET unit transistors

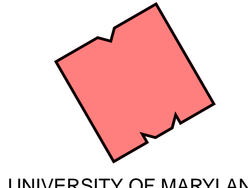


UNIVERSITY OF MARYLAND

ENEE 359a
Lecture/s 3-5
Transistors &
CMOS Inverter

Bruce Jacob

University of
Maryland
ECE Dept.



Long MOSFETs

poly
metal
active
n-well
via

Short
S
G
D

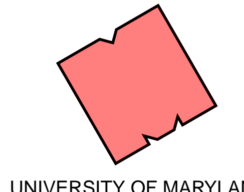
Long
S
G
D

S
D
G

Really Long

Bruce Jacob

University of
Maryland
ECE Dept.



Wide MOSFETs

poly

metal

active

n-well

via

Narrow

S

G

D

Wide

S

G

D

G

S

Really Wide

D

Bruce Jacob

University of
Maryland
ECE Dept.

Transistor Sizing II

Resistance of MOSFET:

$$R_n = \frac{1}{\mu_n C_{ox}(V_{GS} - V_{Tn})}\left(\frac{L}{W}\right)$$

- **Increasing W decreases the resistance; allows more current to flow**

Oxide capacitance $C_{ox} = \varepsilon_{ox}/t_{ox}$ **[F/cm²]**

Gate capacitance $C_G = C_{ox}WL$ **[F]**

Transconductance $\beta_n = \mu_n C_{ox}\left(\frac{W}{L}\right) = k'_n\left(\frac{W}{L}\right)$

(units [A/V²])

Bruce Jacob

University of
Maryland
ECE Dept.

Transistor Sizing II

nFET vs. pFET

$$R_n = \frac{1}{\beta_n(V_{DD} - V_{Tn})} \qquad \beta_n = \mu_n C_{ox}\left(\frac{W}{L}\right)_n$$

$$R_p = \frac{1}{\beta_p(V_{DD} - |V_{Tp}|)} \qquad \beta_p = \mu_p C_{ox}\left(\frac{W}{L}\right)_p$$

$$\frac{\mu_n}{\mu_p} = r$$

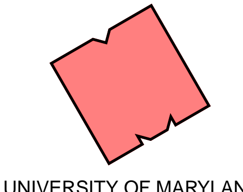
Typically (2 .. 3)

(μ is the carrier mobility through device)

ENEE 359a
Lecture/s 3-5
Transistors &
CMOS Inverter

Bruce Jacob

University of
Maryland
ECE Dept.



Inverter Switching Point

Where Vin = Vout

NMOS off
PMOS res

NMOS sat
PMOS res

NMOS sat
PMOS sat

NMOS res
PMOS sat

NMOS res
PMOS off

2.5
2
1.5
1
0.5
0

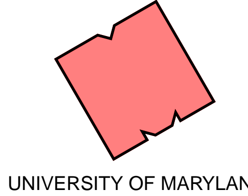
V_{out} (V)

0
0.5
1
1.5
2
2.5

V_{in} (V)

Bruce Jacob

University of
Maryland
ECE Dept.



Inverter Switching Point

At all points $I_{DSn} = I_{DSp}$ (drain currents)

At switching point, Vin = Vout = Vsp

$$\frac{\beta_n}{2}(V_{SP} - V_{Tn})^2 = \frac{\beta_p}{2}(V_{DD} - V_{SP} - V_{Tp})^2$$

$$V_{SP} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} \cdot V_{Tn} + (V_{DD} - V_{Tp})}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

For Vsp = Vdd/2, assuming $V_{Tn} = V_{Tp}$,

$ß_n = ß_p$ => $W_p \approx 2\text{–}3W_n$

(equal drive currents, equal R_{eff}: $R_n = R_p$)

Bruce Jacob

University of
Maryland
ECE Dept.

The Result ($W_p = 2W_n$, .25µm)

In

metal1

metal1-poly via

polysilicon

metal2

V_{DD}

pdiff

PMOS (4/.24 = 16/1)

NMOS (2/.24 = 8/1)

metal1-diff via

ndiff

GND

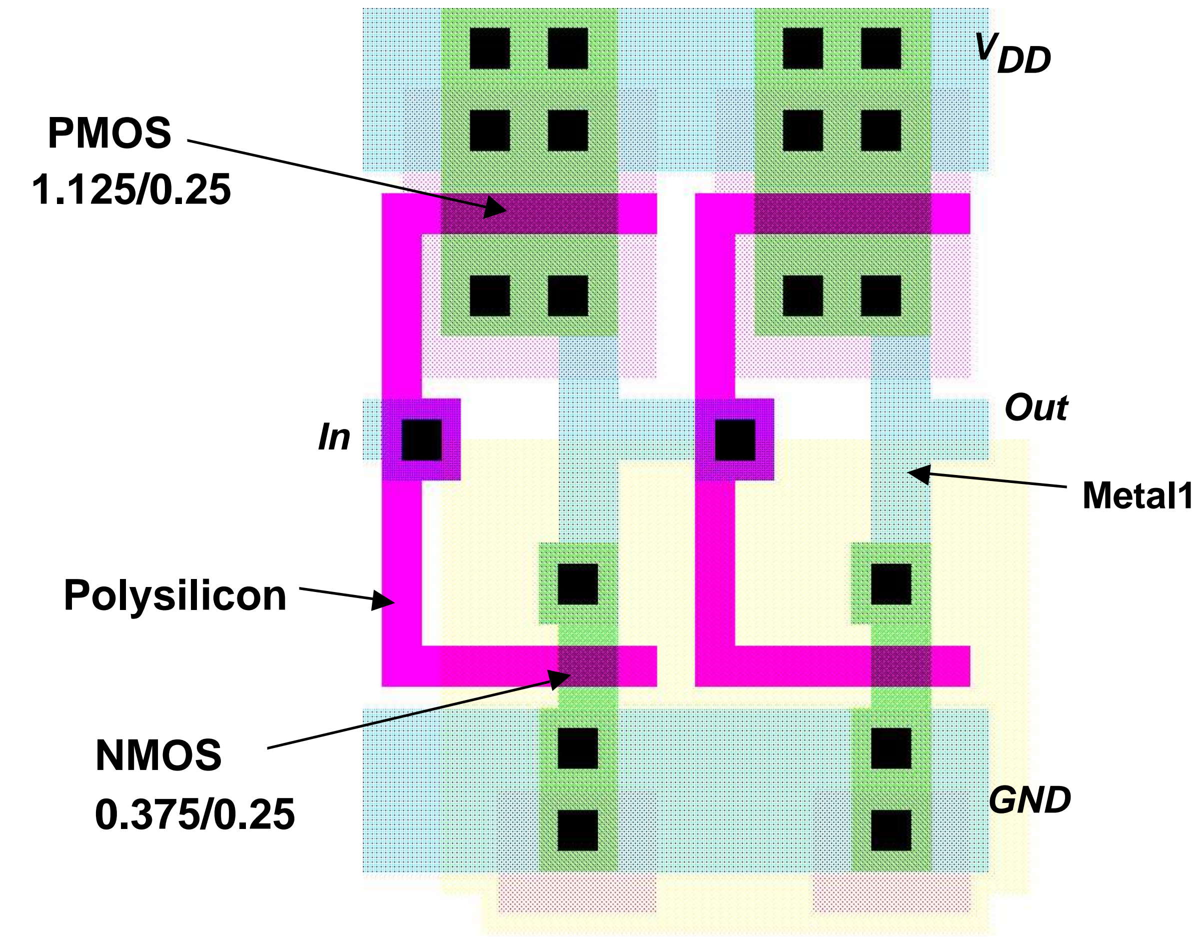
metal2-metal1 via

UNIVERSITY OF MARYLAND

Bruce Jacob

University of
Maryland
ECE Dept.

The Result II ($W_p = 3W_n$)



PMOS devices 3x larger than NMOS devices

UNIVERSITY OF MARYLAND

Bruce Jacob

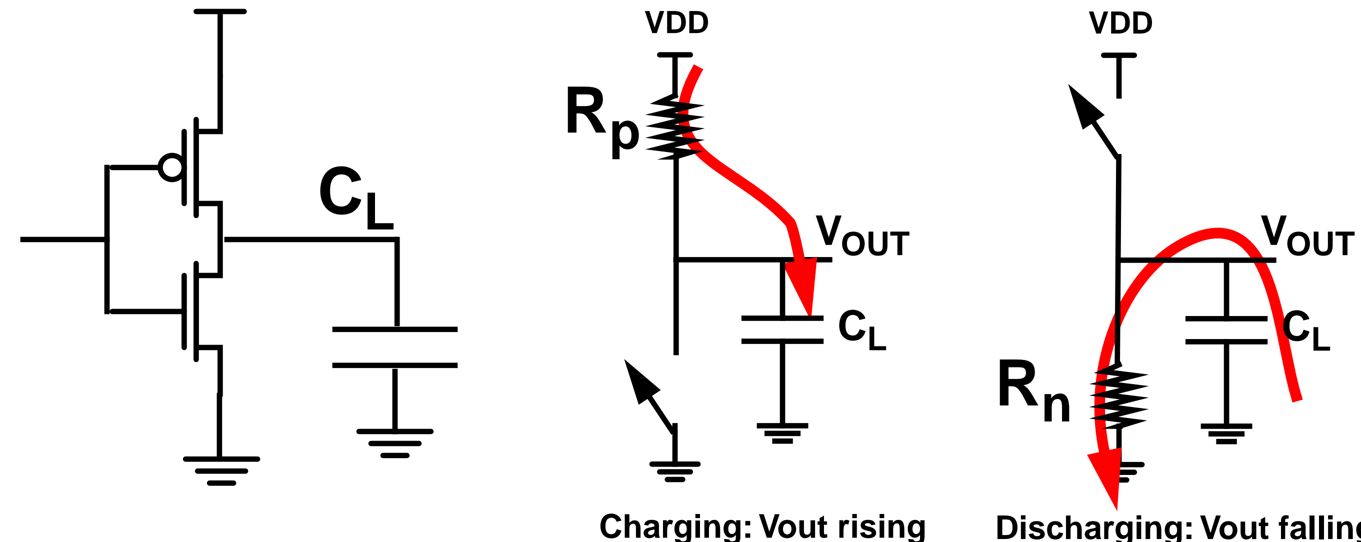
University of
Maryland
ECE Dept.

Delay Definitions

Bruce Jacob

University of
Maryland
ECE Dept.

Inverter Switching Delay



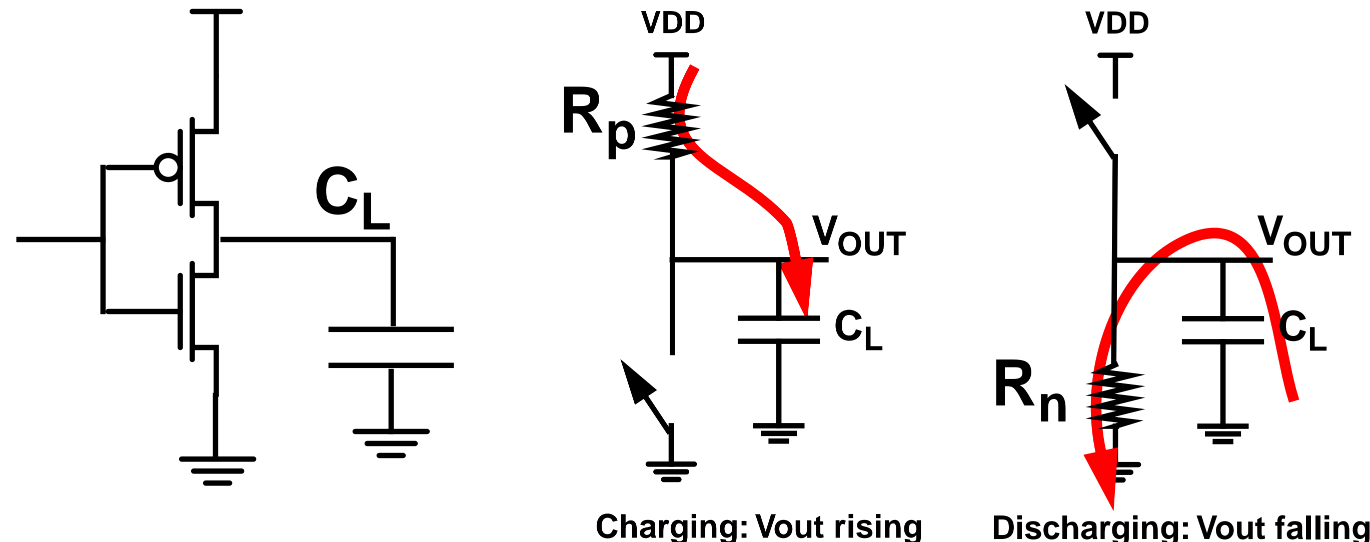
If $(W/L)_p = r(W/L)_n$ then $ß_n = ß_p$
(and $R_n = R_p$)
… symmetric inverter

Make pFET bigger (wider) by factor of *r*

Bruce Jacob

University of
Maryland
ECE Dept.

Inverter Switching Delay



$$t_{pLH} = \ln(2)\, R_p\, C_L = 0.69\, R_p\, C_L$$

$$t_{pHL} = \ln(2)\, R_n\, C_L = 0.69\, R_n\, C_L$$

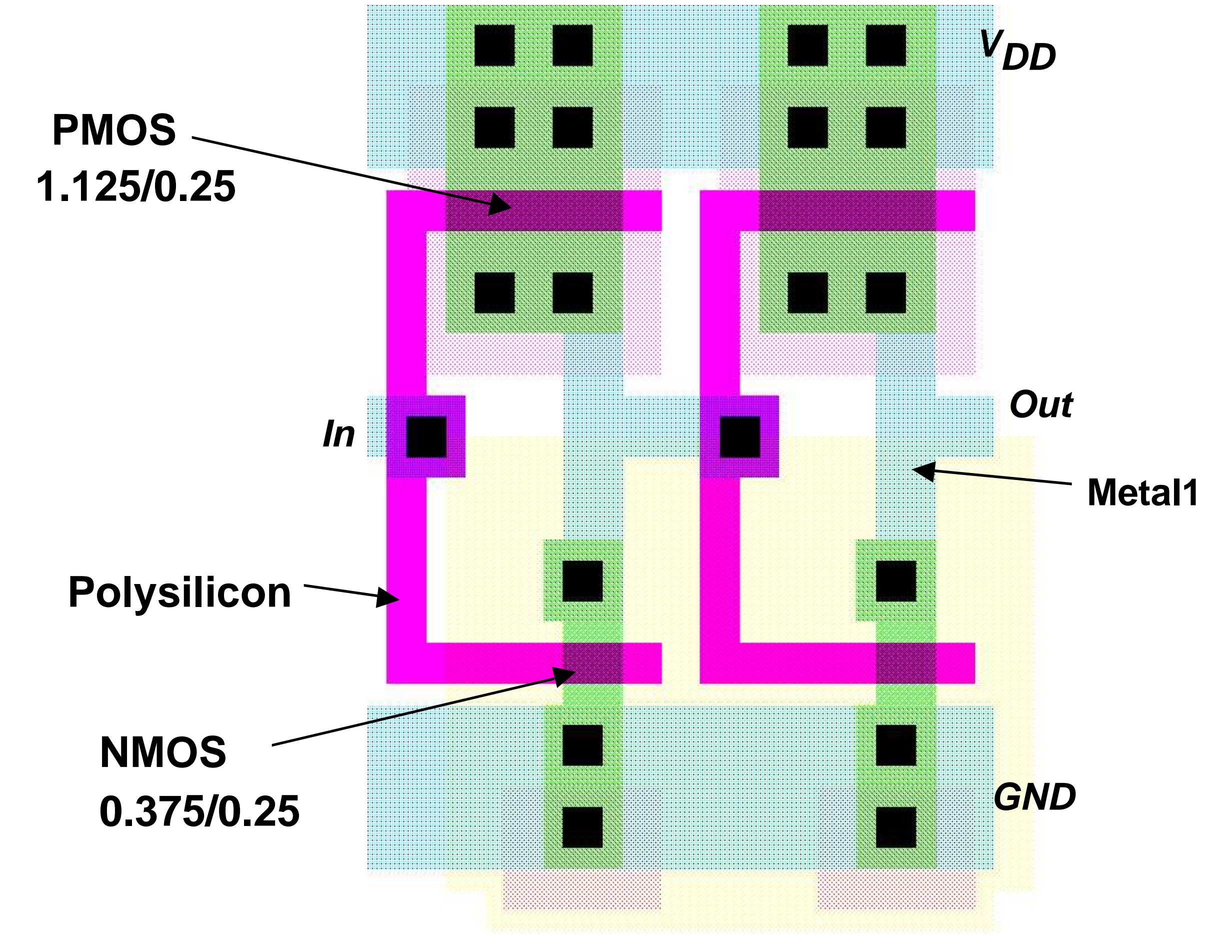
$$t_p = (t_{pHL} + t_{pLH})/2 = 0.69\, CL(R_n + R_p)/2$$

(note: the ln(2)RC term comes from first-order analysis of simple RC circuit’s respose to step input ... time for output to reach 50% value)

Bruce Jacob

University of
Maryland
ECE Dept.

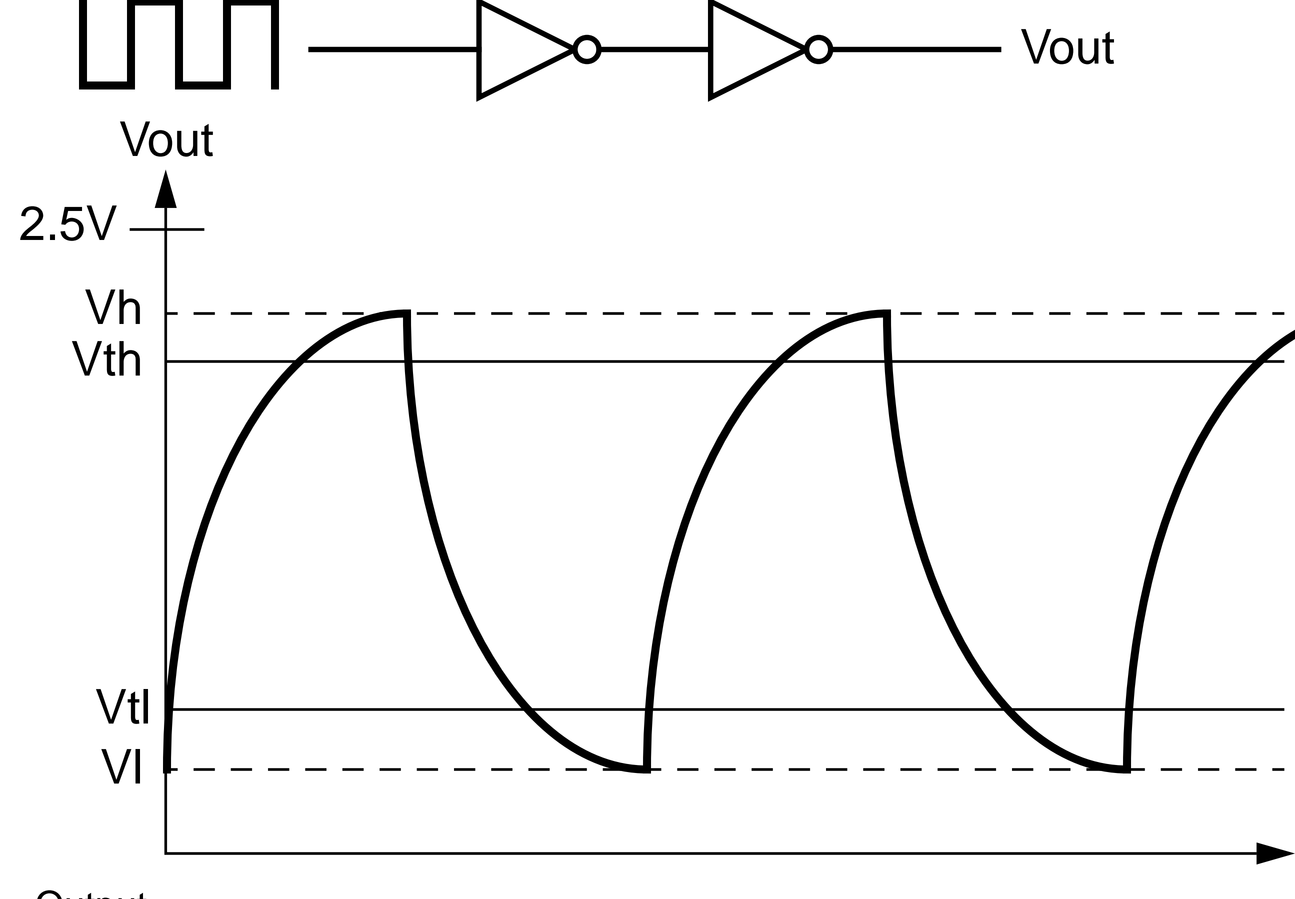
Inverter Pair



Bruce Jacob

University of
Maryland
ECE Dept.

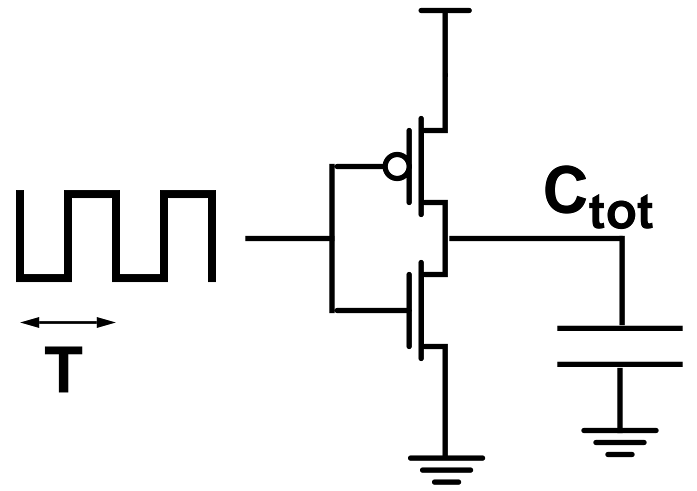
Inverter Pair

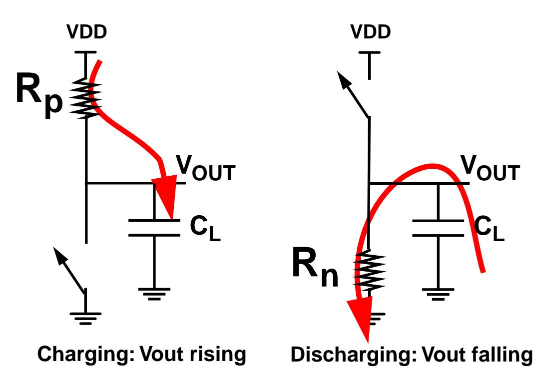


Bruce Jacob

University of
Maryland
ECE Dept.

Dynamic Power Dissipation





$$I_{avg} = \frac{Q_{Ctot}}{T} = \frac{V_{DD} \cdot C_{tot}}{T}$$

$$P_{avg} = V_{DD} \cdot I_{avg} = \frac{C_{tot} \cdot V_{DD}^2}{T} = C_{tot} \cdot V_{DD}^2 \cdot f_{CLK}$$