ENEE 302H, Fall 2004
Digital Electronics

Manufacturing

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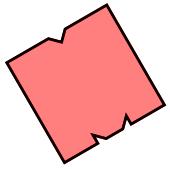

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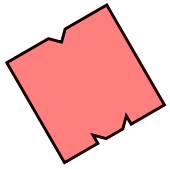
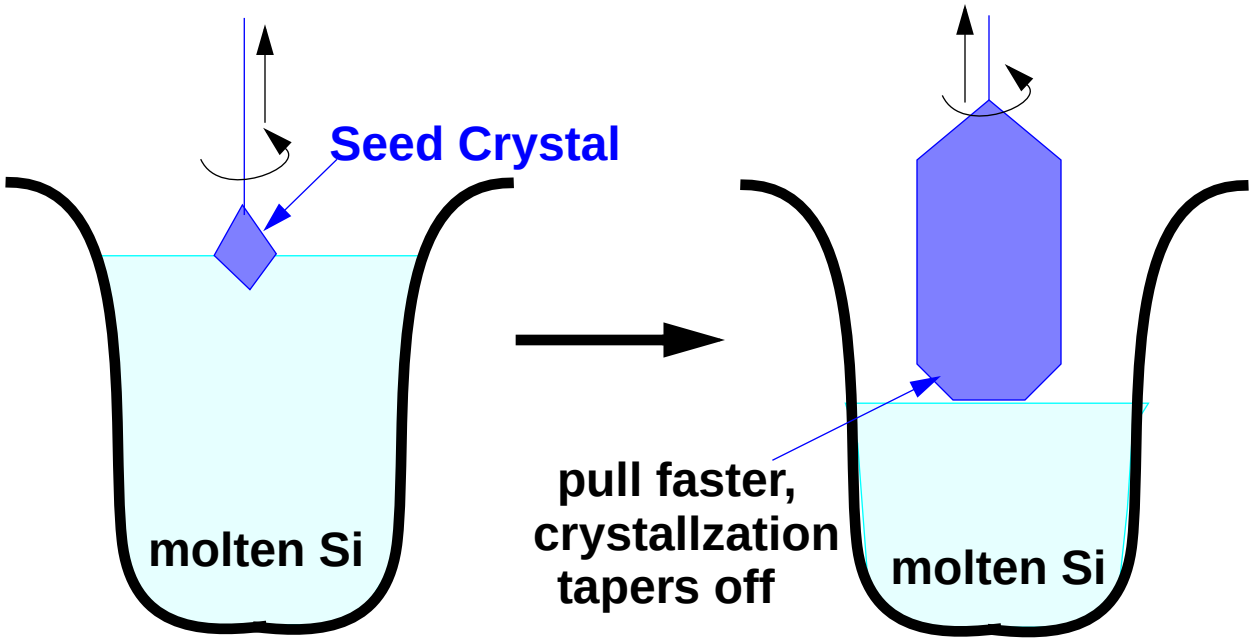
Overview

- **What makes silicon a good base to build on? Why not other stuff? (Discussion: the Silicon CMOS Steamroller)**
- **Wafer preparation. (Bulk, SOI)**
- **Microelectronics Magic**
- **Testing**
- **Packaging**
- **End Product + Show and Tell.**



Wafer Preparation 1:

Silicon Crystal Growth:



An Artist needs canvas to paint.

IBM/Intel/TSMC/Infineon/Micron etc need silicon wafers to build chips.

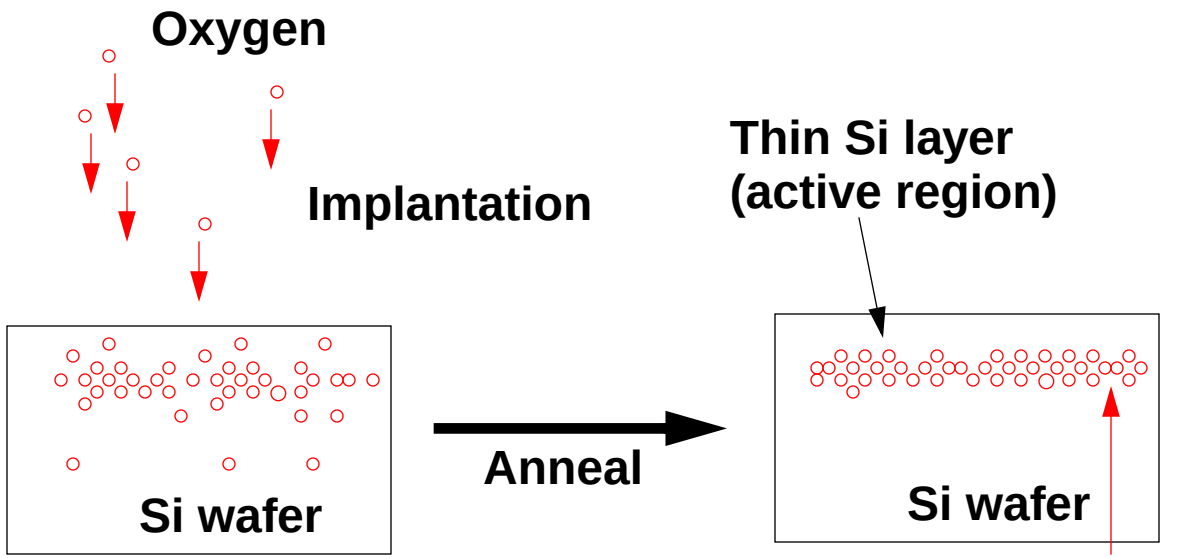
Need to grow single crysal silicon with high purity.

Grow silicon crystal with 200mm or 300mm diameter, then cut wafers.

Vertical speed, rotational speed/torque, temperature, all critical

Wafer Preparation 2:

SOI: Silicon On Insulator



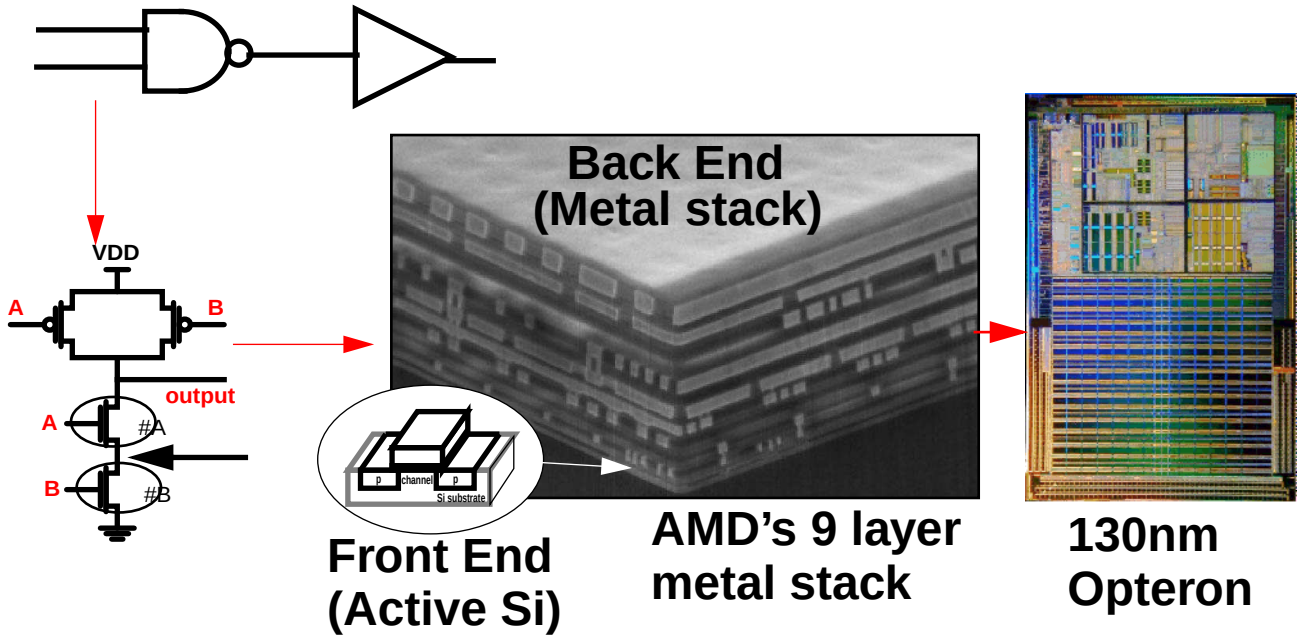
One way to do it. (Not the only way)

Oxygen Implantation and anneal process creates effective BOX.

SOI wafers typically more expensive than bulk (lower yield)

Intel/IBM/TSMC buys wafers from specialized companies.

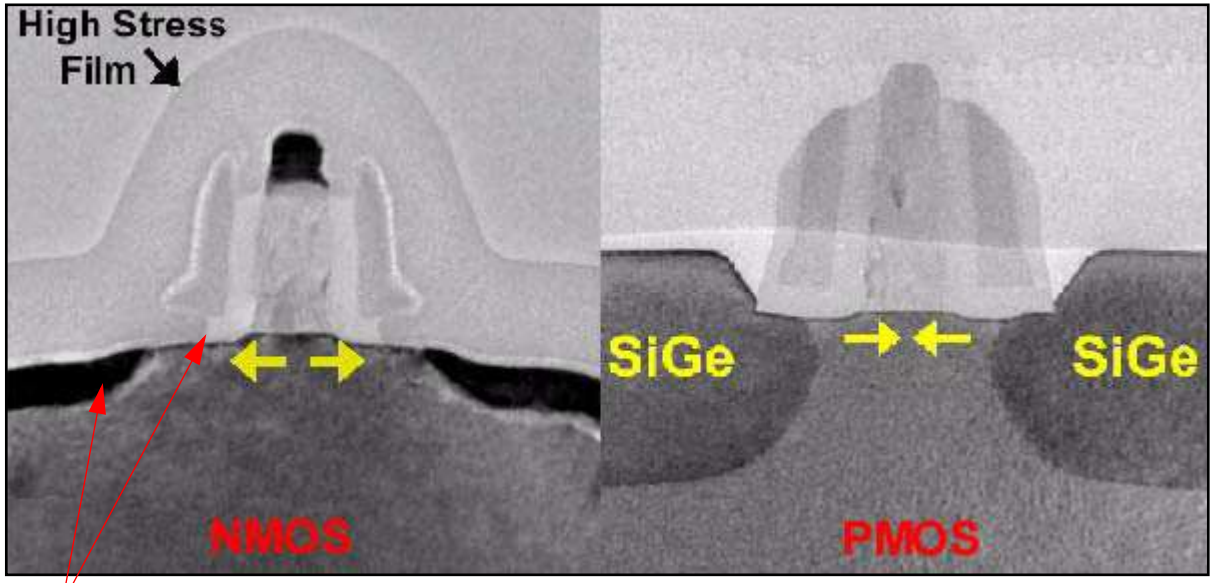
Microelectronics Magic 1:



- Take logic design,
- Translate to circuit design
- Build transistors on active silicon
- Connect transistors
- Get silicon chip: CPU, DRAM, SRAM, Flash, DSP, bio/ chem sensors, communications....

Microelectronics Magic 2:

Building Layers



Fundamentally 3D structures

Intel's strained-Si @ 90nm

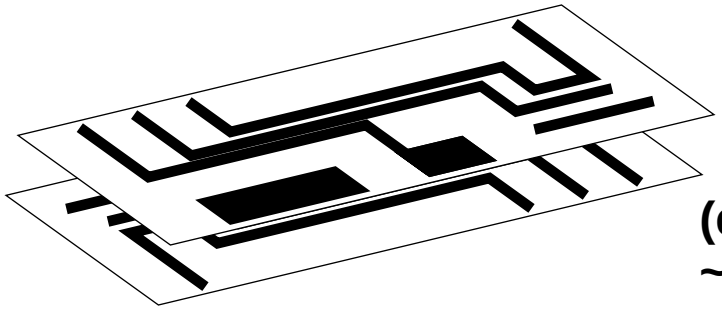
Bottom line: build layers of stuff by adding material or removing material from surface of silicon.

Parallel (Masks and resists, wafer level) or Serial (beams, one line at a time: Ion Beam)

Higher throughput == Lower cost

Material scientists bring new materials into play every generation: Moore's law.

Microelectronics Magic 3:



Mask Set
Very expensive
(especially front end)
~ $1M @ 90nm node*

Discussion:

What is a "class 1 fab"?

What is a "stepping"?

Patterning: creating 3D structures
Future: MEMS?

Adding (converting) material

Spin on
Deposition: CVD
Implantation
Oxidation

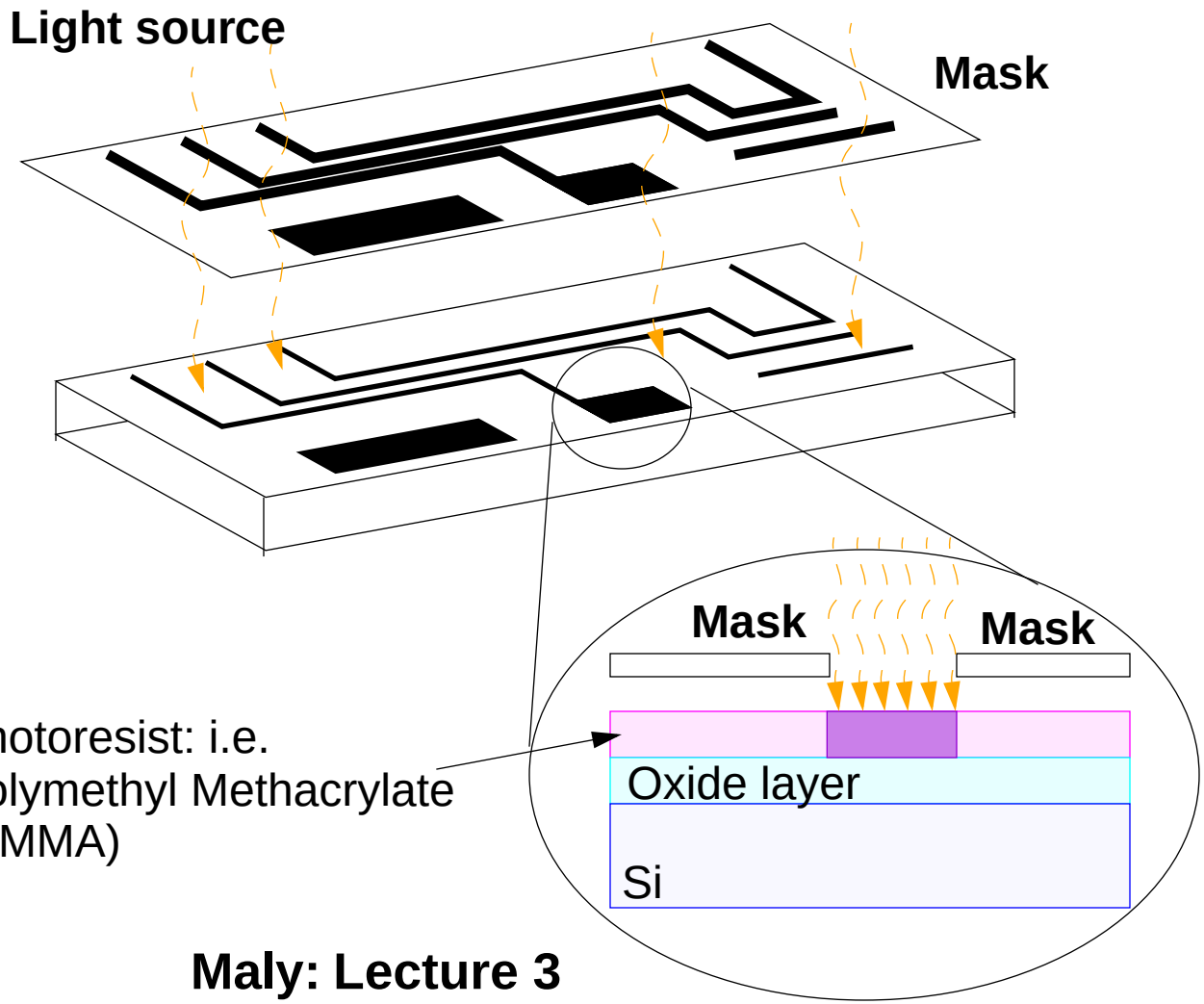
Removing material

Etching
Polishing: CMP
Chemically

CVD: Chemical Vapor Deposition
CMP: Chemical-Mechanical Polishing
***Estimate given by IC Knowledge LLC**

Microelectronics Magic 4:

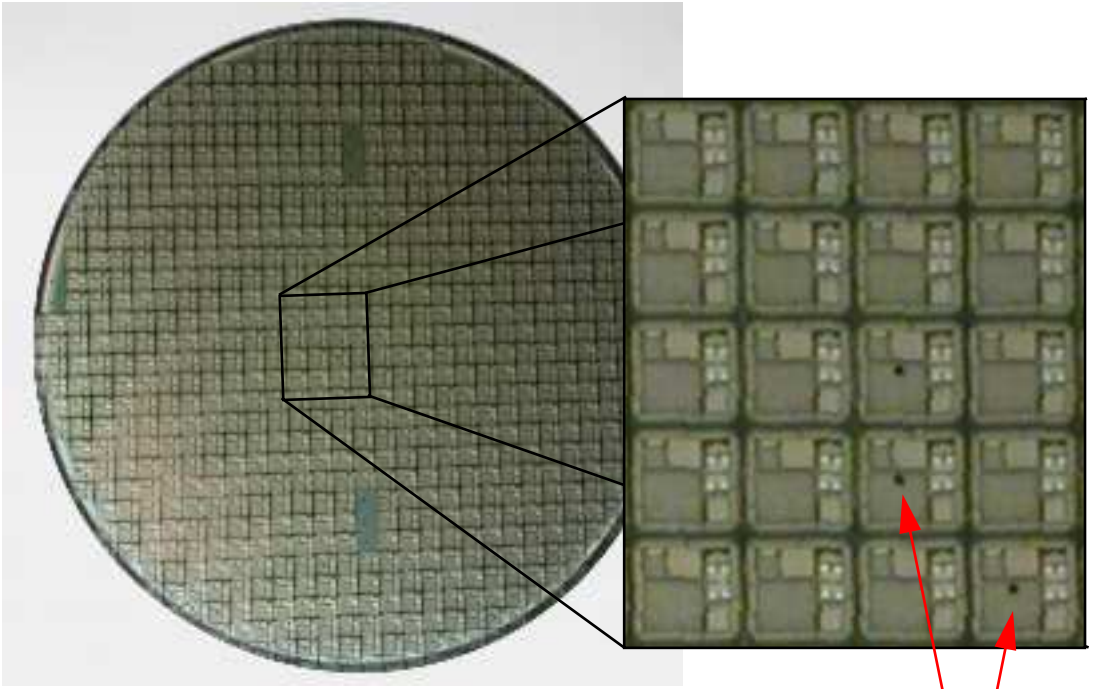
Lithography



Maly: Lecture 3

Testing:

You've made it. Does it work?



Millions of transistors, 100% functional? If not, how do you find the failed one?

Functional Tests

- **Wafer probe**
- **IDDQ**
- **Infrared**
- **BIST**

Packaging:

Connecting chips to each other