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Double Patterning and Hyper-Numerical Aperture Immersion Lithography

In attempt to continue the advancement of fabrication in accordance with Moore's Law, double patterning lithography (DPL) has been introduced. Double patterning lithography does not introduce any new technology and is used because the industry requires it, rather than actually desires to use it [1]. Since no new technology is introduced, it is viewed as a short-term solution. Double patterning lithography is useful in that it will allow fabrication of the 22nm node and beyond [1]. There are several double patterning lithography techniques that have been developed. These techniques are litho-etch litho-etch (LELE), litho-freeze litho-etch (LFLE), and self-aligned double patterning (SADP), each with its own advantages and disadvantages. The most commonly used techniques are LELE and LFLE.

The first double patterning technique, litho-etch litho-etch (LELE), is the most straightforward. It consists of an initial lithography step followed by an etching step and then the same process is repeated to get the final pattern, see figure 1. The negative aspects of this technique are that two masks must be used to create the final pattern. This directly increases the time and cost it takes to fabricate using double patterning because the process steps will be effectively doubled [2]. Another struggle with this technique is small tolerance of the pattern overlay [2]. Because of the small-scale patterns used with DPL, a slight misalignment of the second pattern will cause a notable defect in the final pattern.

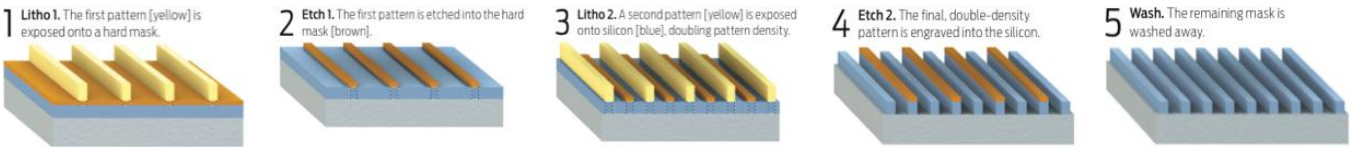

Figure 1. LELE Process [3].

The second technique, litho-freeze litho-etch (LFLE), was introduced to eliminate the increased cost due to additional process steps of the LELE technique. In LFLE there are still two lithography steps, but only one etching step. This can be done through the 'freezing' of the first pattern [2]. The freezing step is implemented in such a way that a chemical treatment is able to alter the initial pattern so that it is unaffected by the exposure and development of the second pattern [2]. Following the development of the second mask, a single etching step takes place. As a result, LFLE is cheaper to perform than LELE, but still faces issues with small pattern alignment tolerances.

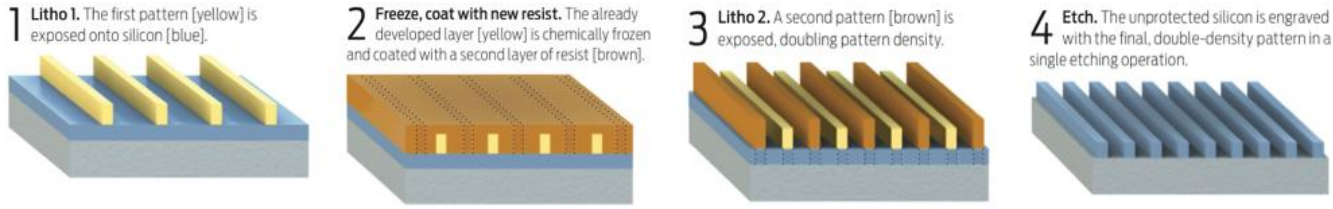

Figure 2. LFLE Process [3].

The technique of self-aligned double patterning (SADP) eliminates the complication of pattern alignment seen in LELE and LFLE [2]. As shown in figure 3, SADP uses an initial photoresist pattern to

determine the spacing of the final pattern, which will be etched. Once the initial photoresist is exposed and developed, a masking material is deposited and etched, forming sidewall spacers. After removing the initial photoresist, the pattern is etched using the remaining sidewall spacers. This technique is more accurate than the first two because it is easier to control pattern dimensions than pattern placement and the use of the initial photoresist pattern fixes the placement of the final pattern leaving only the dimension of the sidewall to maintain. Although it reduces the overlay problems associated with LELE and LFLE, SADP is only suited for uniform patterns for applications such as memory, not logic which is often irregular [2]. Additionally, the cost of this technique is increased with the added process steps used to deposit, etch, and remove the sidewall spacers.

Figure 3. SADP Process [3].

Currently, there is a clear separation in applications of double patterning lithography in the integrated circuit industry. The separation is made between the fabrication of memory and logic. Memory fabrication most commonly uses self-aligned double patterning (SADP) because if its repeating pattern. While logic fabrication is implemented through litho-etch litho-etch (LELE) and litho-freeze litho-etch (LFLE) because of its tendency to have non-uniform patterns. This separation in application of DPL is the reason memory manufacturers such as Hynix, Micron, Renesas, and Samsung utilize SADP. Whereas the IBM partnership companies, Intel, Sony, TI, Toshiba, and TSMC, who manufacture logic devices use LELE and LFLE [2].

Hyper-Numerical Aperture Immersion lithography, on the other hand, is very similar to projection lithography but provides the capability to achieve much higher resolution [4]. The mechanism behind reducing the minimum feature size is directly related to the numerical aperture (NA) of the imaging equipment used [4]. The light source will be a 193nm argon fluoride (ArF) excimer laser and in addition to the conventional projection lithography set up, a highly purified liquid medium is placed between the lens and wafer [5]. The refractive index of this liquid medium will be greater than one and as such, the numerical aperture of the set up will increase as NA= sin(max refraction angle) * refractive index of liquid medium [5]. The addition of the liquid medium to replace what is conventionally an air-gap between the lens and wafer, will result in light that is project through the mask and lens to be redirected with minimal reflection. This will result in much more precise, and smaller feature sizes that are patterned into the photoresist. The depth of focus is greatly increased [6]. The liquid is constantly circulated to help mitigate thermally induced distortions. The setup is show below:

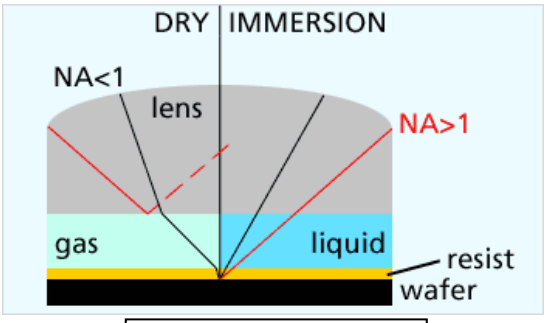

Figure 3. Zeiss [4]

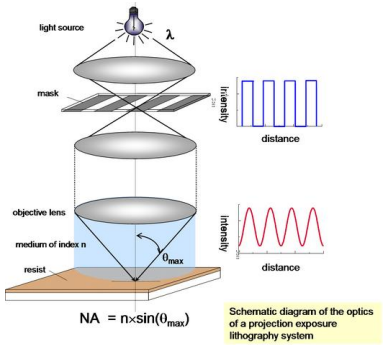

Figure 4. IBM [4]

Figures: Figure 3 is an image comparing the setup between a dry and immersion lithography system in terms of the numerical aperture of the imaging equipment as well as the path of the laser light [5]. Figure 4 is an image of the overall setup for immersion lithography, starting with the laser light source, down to the waver with photoresist [4]. The light blue represents the liquid medium.

The most common liquid medium is highly purified deionized water with an index of refraction of 1.44 will increase the resolution of resolvable feature sizes by a factor of approximately 30% [6]. Depending on the liquid used, increases in resolution can range between 30-40%. Since the liquid is in direct contact with the photoresist on the wafer, optimal lithography will be done using a water resistant photoresist or a protective topcoat on top of the photoresist. This method is a less expensive way to achieve smaller feature sizes without having to take on immense changes in equipment to costly x-ray lithography systems, for example.

However the hyper numerical aperture immersion lithography technique does come with disadvantages as well. Since the liquid medium is in direct contact with the wafer, defects may arise due to bubbles within the fluid as well as temperature and pressure variation in the fluid [6]. The protective photoresist is prone to absorbing the fluid medium. Also, the 193nm excimer laser light can ionize the water medium which can promote reaction with the photoresist and distort the accuracy of desired features [6]. When the wafer is removed from the system, residual water may still remain, causing problems since moisture will effect proper device operation and processing. Finally, this method can be more expensive than dry, conventional lithography since the apparatus requires extra apparatus' as well as meticulous maintenance.

Industry leaders such as Intel, Texas Instruments, etc. are utilizing hyper numerical aperture immersion lithography systems to be able to achieve smaller and smaller feature sizes. When combining this method with double patterning, many of these companies are able to achieve critical dimensions of around 25nm [6]. Node sizes of transistors made by companies like Intel, Toshiba, IBM, and AMD are around 32nm and 22nm with the help of hyper-numerical aperture immersion lithography systems. Hence this technology is assisting Intel and companies in the like to keep up with Moore's Law projections. Nikon, Cannon, and ASML are known to actually manufacture such immersion lithography equipment.

References

[1] P. Zimmerman, “Double patterning lithography: double the trouble or double the fun,” SPIE Newsroom, [Online]. Available: http://spie.org/documents/Newsroom/Imported/1691/1691_5999_0_2009-06-24.pdf
[2] C. Mack, “Seeing Double,” IEEE Spectrum, November 2008, [Online]. Available: http://spectrum.ieee.org/semiconductors/design/seeing-double/0
[3] “All Double-Patterning Variations Lead to Rome,” IEEE Spectrum, [Online]. Available: http://spectrum.ieee.org/images/nov08/images/doub03.pdf
[4] “Immersion Lithography,” IBM, [Online]. Available: http://www.almaden.ibm.com/st/chemistry/lithography/immersion/
[5] “Optics for 193nm Immersion Lithography,” Carl Zeiss, [Online]. Available: http://www.zeiss.de/c12567b0003c017a/Contents-Frame/0358803766924803c12567b0003d5d3f
[6] B.W. Smith, Y. Fan, M. Slocum, L. Zavyalova, “25nm Immersion Lithography at a 193nm Wavelength,” Rochester Institute of Technology, Proceedings of SPIE, SPIE Microlithography, Optical Microlithography XVIII, Immersion Lithography, 5754, San Jose, California, United States, pp. 141-147 (2005).