MIC-2 Control Signals														
OpCode Decimal	Mnemonic	ALU F1	ALU F0	SHFT S1	SHFT S0	Latch NZ	AMUX	ENC AND	MAR	MBR	RD	WR	COND C1	COND C0
0	ADD					+		+						
1	AND		+			+		+						
2	MOVE	+				+		+						
3	COMPL	+	+			+		+						
4	LSHIFT	+		+		+		+						
5	RSHIFT	+			+	+		+						
6	GETMBR	+				+	+	+						
7	TEST	+				+								
8	BEGRD	+							+		+			
9	BEGWR	+							+	+		+		
10	CONRD	+									+			
11	CONWR	+										+		
12														
13	NJUMP	+												+
14	ZJUMP	+											+	
15	UJUMP	+											+	+

Control signals generated by the opcode decoder for each mic2 microinstruction opcode. Note: A plus means the signal is asserted (i.e., set equal to 1); a blank means it is negated (i.e., set equal to 0). The two clocked D-latches used to remember the N and Z signals coming from the ALU are controlled by the "Latch NZ" signal, which is ANDed with timing signal T4; so that if the Latch NZ signal is asserted (i.e., equal to 1) and it is timing phase T4, then the clock line into the N and Z latches goes to logic 1 and these latches copy and hold the ALU's N and Z signal values, respectively, for later use by either a ZJUMP or NJUMP microinstruction. The Latch NZ control signal generated by the opcode decoder and the addition of the N and Z latches are the main differences between the mic2 and the mic1; the remaining 12 control signals generated by the mic2's opcode decoder are the same as those used to control the mic1's data path and, thus, perform the same functions as those specified in the Microinstruction format (32-bit word) for the mic1.