Modern Superscalar Case Study

from Palacharla, Jouppi, and Smith - ISCA '97

Fetch Decode Rename Issue Register Read Execute Memory Commit

Example Pipeline (Similar to MIPS R10000, DEC 21264)
Register Renaming

Renaming 1 instruction:

- Register File:
  - R0
  - R1
  - R3
  - R31
  - R127

- Free List:
  - R20
  - R14
  - R32
  - R16
  - R32

- Current Map:
  - ADD R1 R2 R3
  - R0: R0
  - R1: R18
  - R2: R47
  - R3: R19

- Committed Map:
  - ADD R1 R23 R47 R19
  - R0: R0
  - R1: R18
  - R2: R47
  - R3: R19

Renaming Multiple Instructions:

- Current Map
- Source Regs. (Architectural)
- Destination Regs. (Physical)
- Renamed Regs. (Physical)
- Dependence Check Logic
- Source Register (Architectural)
Issue

Wake up Logic:

Select Logic:

Instruction Window

Arbitration Logic
Commit

- Commit instructions in-order.
  - Check exceptions
  - Update Committed Map
  - Update memory

- Maintain slots as a circular buffer
  - Commit instructions from head.
  - Allocate slots from tail.