Student Paper

Analysis of the Biasing Conditions and Latching Operation for Si/SiGe Resonant Interband Tunnel Diode Based Tunneling SRAM

S. Sudirgo[a], D.J. Pawlik[a], S.L. Rommel[a], S.K. Kurinec[a], P.E. Thompson[b], and P.R. Berger[c]

[a] *Rochester Institute of Technology, Department of Microelectronic Engineering, USA, ssudirgo@mail.rit.edu*
[b] *Naval Research Laboratory, USA,*
[c] *The Ohio State University, Department of Electrical Engineering, USA*

A memory cell utilizing negative differential resistance (NDR) characteristic of tunnel diodes was first proposed by Goto *et al.* in 1960 [1]. The inherently fast tunneling phenomenon and low power consumption makes this type of memory architecture attractive. Combined with the possibility for vertical integration of the tunnel diode directly atop of the source/drain region of the FET, a compact design can be achieved. The concept was further refined by Van der Wagt *et al.* to achieve low stand-by power by utilizing diode junction capacitance to lower peak and valley current densities. Utilizing InP/InGaAs resonant tunnel diode (RTD), a nA operation was realized [2]. The realization in Si-based system, however, is still limited. Utilizing p^+Si/oxynitride/n^+poly Si tunnel diodes, Morimoto *et al.* demonstrated a low voltage T-SRAM [3]. The performance was limited by the poor performance of the tunnel diode and the lack of capability to scale current density and size. In recent work by the authors, Si/SiGe resonant interband tunnel diodes (RITDs) have been successfully integrated with CMOS devices. A low voltage monostable-bistable logic element (MOBILE) latch has been demonstrated [4]. The current density of a Si/SiGe RITD is controlled by adjusting the SiGe i-layer thickness, making it suitable for circuit integration with CMOS [5]. In this work, Si/SiGe RITD-based T-SRAM cell is bread-boarded and its latching mechanisms have been investigated extensively.

As shown in Fig. 1(a), each T-SRAM cell consists of two tunnel diodes connected in series with a current manipulator, NFET, connected into the sense node. In this experiment, Si/SiGe RITDs with 6 nm i-layer grown on top of p^+ implanted wells with PVCR of 2.25 and peak current density of 2.15 kA/cm^2 were used. During the stand-by (SB) mode, NFET is off, and V_{DD} is fixed at 1.0V, as illustrated in Fig. 1(b). RITD1 and RITD2 function as the driver and load, respectively, resulting in folded current-voltage characteristics as depicted in Fig. 2. The intersections the drive and load curves indicate two stable latching states, stand-by low (SBL) and high (SBH) at 246 mV and 746 mV, respectively. These two states represent logic low and high, respectively. It is important to note that the intersection at the negative differential resistance (NDR) region is unstable and is not be used as a latching point.

To latch into logic high, a current has to be supplied into the sense node through the NFET by applying a bias of 2.0V to both the drain and gate. Fig. 1(c) depicts the circuit diagram during this write high (WH) cycle. By activating the NFET, a current path parallel to RITD2 is formed, elevating the overall current that passes through the load diode as shown in Fig. 3. At the same time, current injection into the middle node also causes a decrease in drive current. As a result, the potential at the sense node (V_{SN}) changes abruptly from point **A**, 246 mV, to **B**, 802 mV. By restoring the stand-by biasing conditions, i.e. shut-off the NFET, V_{SN} restores to the nearest stable latching state at 746 mV, point **C**.

In the write to logic low (WL) cycle, current is subtracted or drained from the sense node by simply applying a bias to the gate of the NFET and grounding the bit node. Since there is a potential difference between sense and bit node, current will flow out of the sense node as illustrated in Fig. 1(d). In other words, a current path parallel to RITD1 is created, causing a rise in the drive current. Unlike the write high cycle, the load characteristic is undisturbed during WL cycle. As a result, V_{SN} changes suddenly from point **C**, 746 mV, to **D**, 199 mV (Fig. 4). Restoration to the stand-by conditions shifts the latching point back to **A**, 246 mV. The corresponding time diagram of write and read cycles is given in Fig. 5. Slight discrepancies between the values from I-V curves and transient diagram is due to parasitic resistance present in the test setup.

In conclusion, a prototype of Si/SiGe RITD-based T-SRAM has been presented. Load line analysis is performed to understand the latching mechanisms during the write and read cycles. This demonstration will lead to realization of fully-integrated Si/SiGe RITD/NMOS T-SRAM. Ultra-low power tunneling SRAM can be achieved by utilizing low current density RITDs.

References

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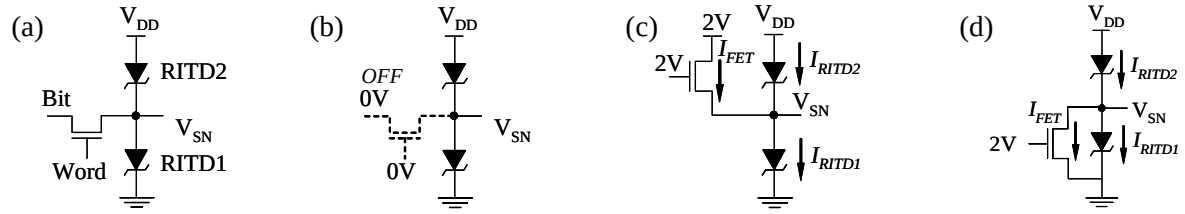

Fig. 1 Circuit diagram of (a) T-SRAM cell; (b) during stand-by mode; (c) during the write to logic high (WH) cycle; (d) during the write to logic low (WL) cycle.

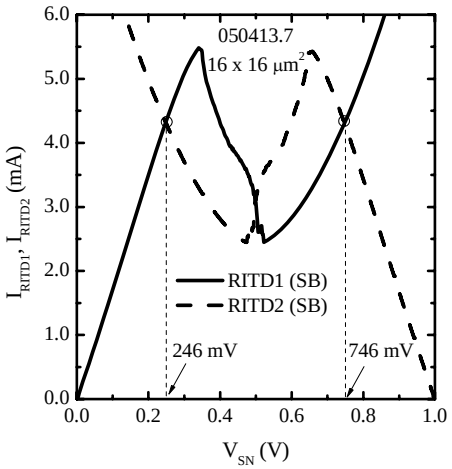

Fig. 2 Load line analysis of T-SRAM cell during stand-by (SB) mode, illustrating two latching points.

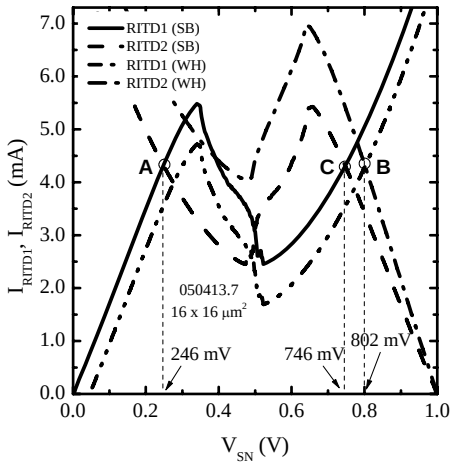

Fig. 3 Load line analysis during write to logic high (WH) cycle, from point **A** to **B** to **C**.

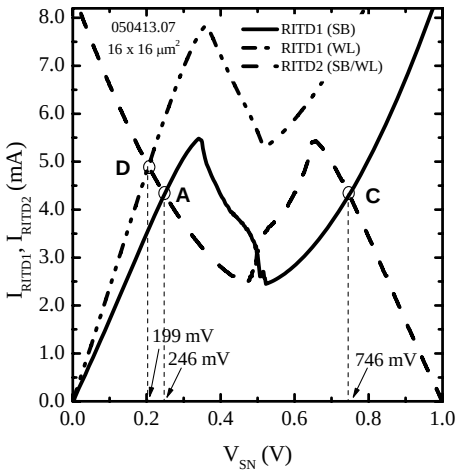

Fig. 4 Load line analysis during write to logic low (WL) cycle, from point **C** to **D** to **A**.

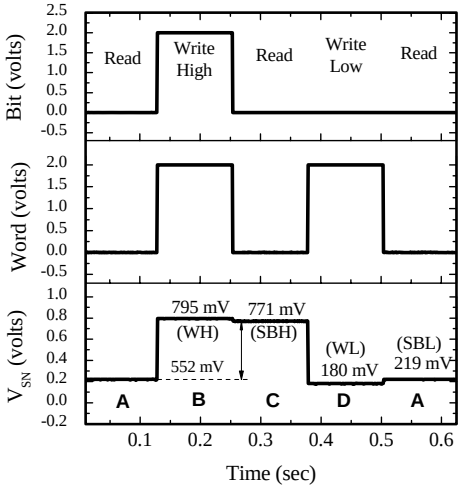

Fig. 5 Time response diagram of T-SRAM at different stages of read and write cycles.