High Temperature Capping Layers for SiC Based Devices

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Motivation

With the collaboration of the Army Research Laboratory and the University of Maryland, research to design a lighter, faster hybrid tank is currently being initiated. These tanks require millions of electronic devices such as MISFETS, GTO thyristors and diodes. Silicon based semiconductor cannot withstand the heat, therefore silicon carbide based semiconductors are being investigated.

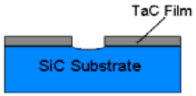
GTO thyristors, MISFETS and diodes

Why Silicon Carbide?

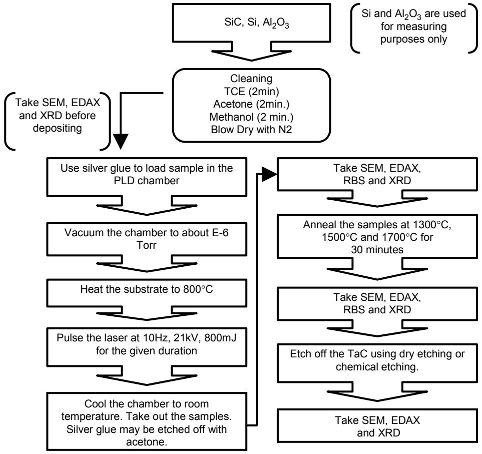
- Application in high heat and high power electronics
- High breakdown voltages
- Low resistance → reduce drift region with due to high band gap
- High switching frequency → device switches faster
- Smaller heat sinks – thermal conductivity of SiC is three times greater than silicon → better heat dissipation → results in reduced thermal management system

Why Tantalum Carbide?

- High temperature stability and high melting point
- Possibility to act as a mask for various doping processes
- Does not react with hydrogen during selective growth process



Experimental Procedure



SiC, Si, Al_2O_3

Si and Al_2O_3 are used for measuring purposes only

Cleaning
TCE (2min)
Acetone (2min.)
Methanol (2 min.)
Blow Dry with N2

Take SEM, EDAX and XRD before depositing

Use silver glue to load sample in the PLD chamber

Vacuum the chamber to about E-6 Torr

Heat the substrate to 800°C

Pulse the laser at 10Hz, 21kV, 800mJ for the given duration

Cool the chamber to room temperature. Take out the samples. Silver glue may be etched off with acetone.

Take SEM, EDAX, RBS and XRD

Anneal the samples at 1300°C, 1500°C and 1700°C for 30 minutes

Take SEM, EDAX, RBS and XRD

Etch off the TaC using dry etching or chemical etching.

Take SEM, EDAX and XRD

Figure 1. Flow diagram for experimental procedure and preparation.

Pulse Laser Deposition (PLD)

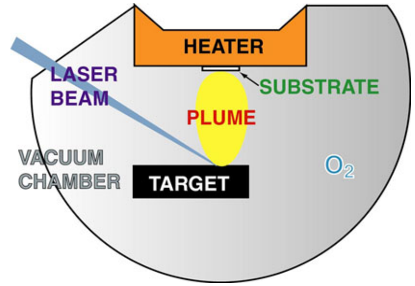


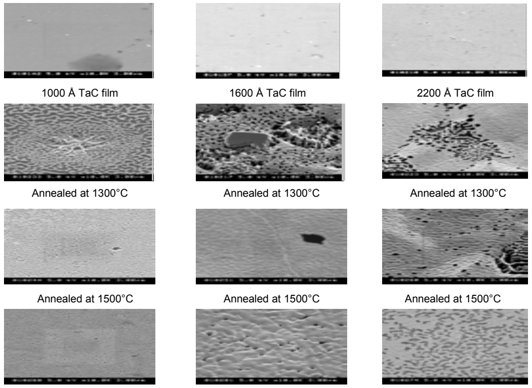
Figure 2 Schematic of PLD Chamber for TaC deposition

Ion Implantation

The dopant atoms damage the lattice structure at the surface of the SiC. Along with the damaged surface, the dopant atoms are not at electrically active locations after implantation. In order to align the implantation, annealing will be performed for thirty minutes at 1300°C, 1500°C, and 1700°C.

Pulse Laser Deposition

While annealing at high temperature is necessary for dopant activation, it brings about further problems with surface morphology. When heated at 1400-1500°C, silicon evaporates, changing the surface stoichiometry. To prevent this, a temperature resistant cap is used. PLD is used to deposit a TaC film. The system (Fig.2) consists of high energy excimer laser that is directed with optics into a vacuumed chamber. The laser strikes the TaC target ejecting a plume of plasma that coats the substrate.



1000 Å TaC film
1600 Å TaC film
2200 Å TaC film

Annealed at 1300°C
Annealed at 1300°C
Annealed at 1300°C

Annealed at 1500°C
Annealed at 1500°C
Annealed at 1500°C

Annealed at 1700°C
Annealed at 1700°C
Annealed at 1700°C

Figure 3 SEM of TaC film before annealing (top row) and after annealing (bottom three rows)

Results and Discussion

- Damaged surfaces of the TaC film after annealing (shown in Fig.3) suggests changes in the morphology and chemical composition of the material.

- The grain growth developed by annealing may be due to contaminant from outside sources or by the chemical and physical properties of TaC when having contact with SiC.

- Results of the XRD shown in Fig. 4 shows the crystalline TaC on SiC.

- The EDAX and RBS results reveals contamination due to oxygen. Figure 5 shows elemental compound percentage of SiC samples.

- To minimize oxygen contamination, a methanol based PLD chamber can be utilized along with using HF as another source of ridding contaminate prior to loading the substrate into the chamber. Carbonizing tantalum deposited on SiC is another technique for deposition.

- Multilayer capping technique can also be used. By capping the SiC with AlN first, then again with TaC reduces strain caused by the crystalline structure of the materials. Also, AlN is compatible with SiC. Etching the TaC off AlN might suggest less surface damage by dry etching.

Conclusion

The analysis shows defects on the surface morphology after annealing. This was the result of oxygen contamination along with the physical and chemical property from the contacts between TaC and SiC. Further investigation in their material properties are being researched. Multilayer capping with AlN and TaC is a promising alternative to reduce strains caused from material contacts along with desired epitaxy.

TaC on SiC

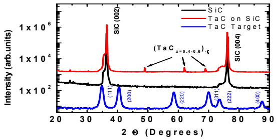


Figure 4. X-ray Diffraction of TaC on SiC before annealing

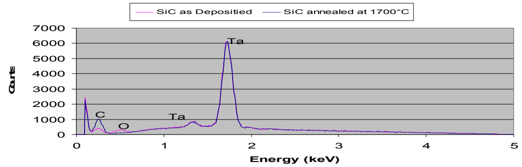


Figure 5 EDAX of TaC on SiC after annealing

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