Introduction

- Need for new development of architecture:

  With the dynamic nature of communication engineering and signal processing, the necessity for flexible and rapidly reconfigurable computing architectures is essential for further growth in the field.

- Design Goal - New architecture:

  Design a fine-grain reconfigurable computing architecture based on a basic cell containing serially settable Look Up Tables and memory capability.

- Design Methodology - Bottom Up:

  Design full-custom layouts to maximize speed and versatility while minimizing chip area and power consumption.

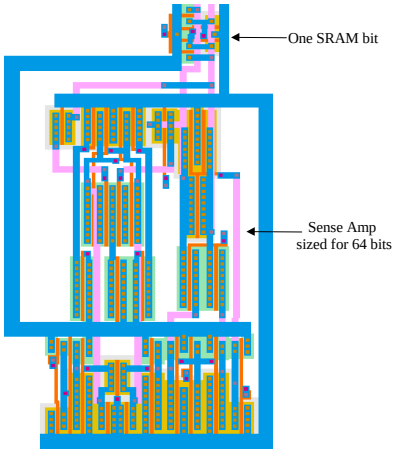
Design Concerns

- Minimizing wire area to cell area ratio.
- Universal signal routing, serial data clock control, and use of logic to reduce control wiring
- Power Consumption in LUTs
- Design of SRAM Sense Amplifier.
- Utilization of Plastic Cell as memory and logic.
- Serial versus Parallel memory and LUT write/read.
- Creating a Stable but dynamically reconfigurable platform.
- Comparison with Current FPGA technology.

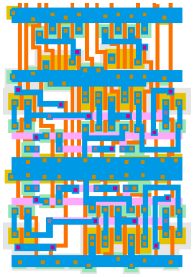
PCA Overview

Plastic Cell Architecture consists of a variable part called the “plastic part” and a fixed part called the “built-in part” arranged in an orthogonal array. The Plastic Part consists of a 4x4 array of Plastic Cells, each consisting of 4 identical LUT memories. A cell can implement a register, any logic function with up to 3 input variables, or routing resources.

SRAM Layout

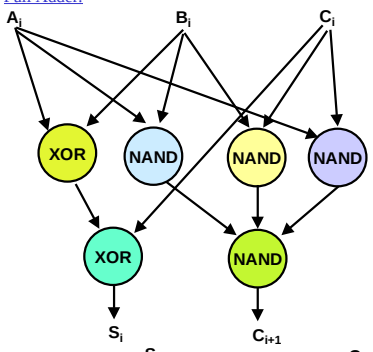


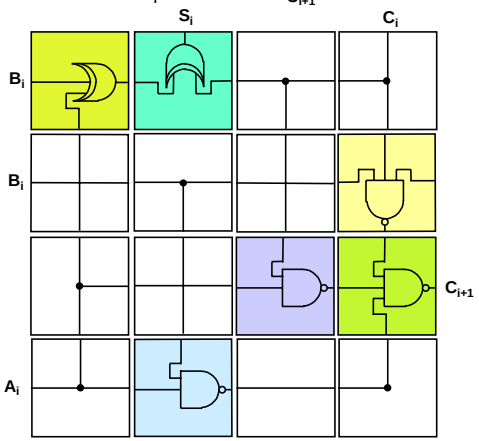
Shift Register Layout



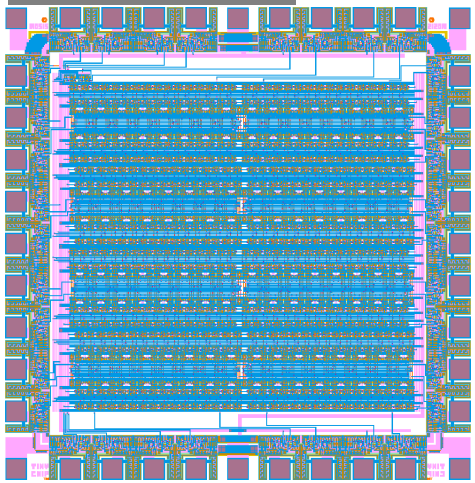
Implementation

Full Adder:





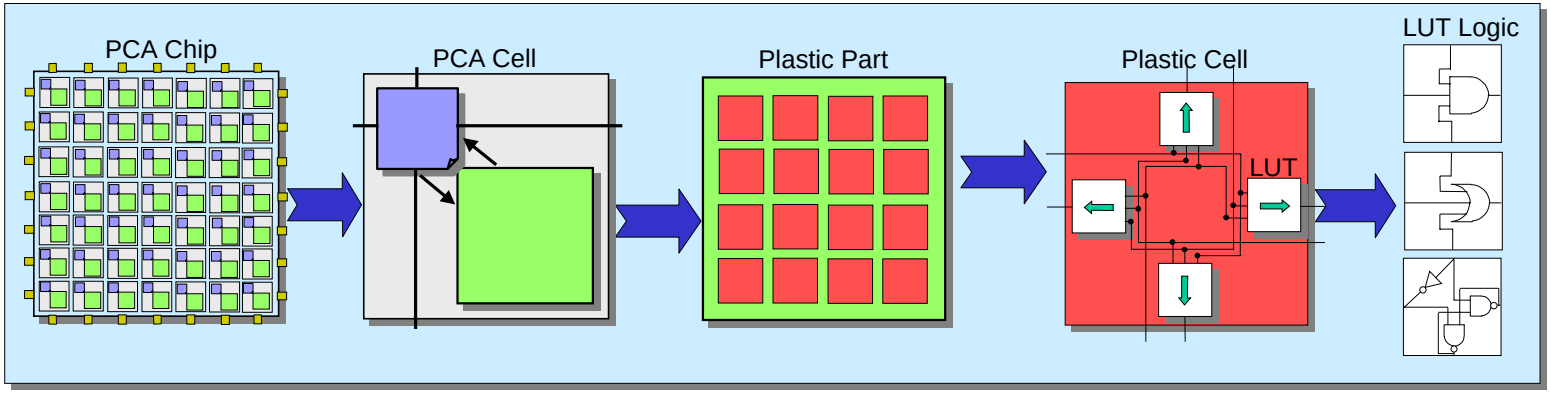
Cell Layout



MOSIS 2 micron Layout of 8 PCA Cells

Functional Comparison

FPGA	2^4 Combinations
PCA	2^{32} Combinations



Conclusion

- Research and Design to Date:
  - VLSI Design and Logic testing on several individual PCA cells. These were sent for fabrication through MOSIS. (1.2micron process)
  - Initial Architecture simulation to maximize cell utilization for functional circuits (Simulated Annealing Programs).
  - Addressed issues of control and data routing for PCA cell.
- Ongoing Work:
  - Verification and Testing of Fabricated MOSIS chips.
  - Development and testing of fully operational PCA chip.
  - Verilog/VHDL migration to PCA programmable routing language.
  - PCA implementation of communication algorithms (FIR Filters, DSP interfaces).