Thermal considerations in High Power Semiconductor Lasers and Semiconductor Optical Amplifiers

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ABSTRACT
In this paper we describe empirical models for predicting the performance of high power lasers, semiconductor optical amplifiers, and superluminescent diodes. The utility of the models is verified by comparing predicted results to actual performance of devices. Based on the model, three important parameters are identified for improving the performance of high power devices. These parameters include reducing the thermal resistance, reducing the series resistance, and reducing the vertical carrier leakage. A method is described to measure the thermal resistance. We further describe experiments done to reduce the series resistance of devices to achieve a value of less than 0.5 $\Omega$ for a 1 mm long ridge device. Finally the effect of carrier stopper layers is described to reduce vertical leakage of carriers.

Keywords: High power lasers, semiconductor optical amplifiers, superluminescent diode, thermal modeling.

1. INTRODUCTION
Many military and commercial applications exist for high power lasers and superluminescent diodes (SLD) that operate in the eye safe spectral region ($\lambda > 1.5 \, \text{mm}$). These include target identification in 3D laser radars, ultra-high power lasers for missile defense systems, free-space line-of-sight communication, and laser machining in manufacturing. There has been considerable effort recently to increase the optical power of lasers and SLDs [1,2]. The design requires careful selection of active region, p and n doping, waveguiding structure and thermal heatsinking. Recently, there have been efforts to simulate the performance of these lasers in high thermal loads [3] using self-consistent models for optical, electrical and thermal characteristics. However, these models are very complex and matching of simulated results with experimental data is difficult. In this paper we describe very simple empirical models to couple separate thermal, optical and electrical models to predict the performance of high power lasers, SLDs and semiconductor optical amplifiers. Good agreement with experimental data is observed. Further important parameters like thermal resistance, series resistance and internal quantum efficiency are identified and experiments done to characterize and improve them are described.

The paper is organized as follow. In Section 2, we describe the empirical model that was constructed for lasers. Predicted light versus current (LI) characteristics are compared with experimental data. Section 3 describes the model for SOAs and SLDs where the carriers are not clamped. Section 4 describes a way to measure the thermal resistance of SLDs and SOAs by comparing CW and pulsed LI characteristics at different heat sink temperatures. Section 5 describes experiments conducted to optimize the doping profile so that the resistance of the device can be reduced. Section 6 summarizes the use of special carrier confinement layers to improve the carrier capture by the active region especially under high carrier concentration. Finally, the paper is summarized in Section 7.

2. EMPIRICAL MODEL FOR LASERS
The total quantum efficiency (also known as wall-plug efficiency), $\eta_{\text{tot}}$ of a diode laser can be defined as the optical power emitted by the semiconductor laser divided by the electrical power applied to the laser to produce this optical power. This value can be conveniently written as a function of the current, $I$, applied to the diode through an external source,
\[
\eta_{\text{tot}}(I) = \frac{P_{\text{opt}}}{P_{\text{el}}} = \frac{S \cdot Ro(I) (I - I_{\text{th}})}{V(I) \cdot I},
\]

where \( S = \Delta P_{\text{opt}}/\Delta I \) is the laser slope efficiency in the small-signal regime, \( Ro(I) \) is a number smaller than one which accounts for the rollover of the optical power (due to thermal self-heating, non-radiative processes like Auger processes and various current leakages), \( V(I) \) is the forward voltage through the laser diode and \( I_{\text{th}} \) is the threshold current. For currents in the diode corresponding to voltage above the turn-on voltage of the diode, we may write

\[
V(I) = V_{\text{turn}} + I \cdot R_s
\]

where \( V_{\text{turn}} \) is the turn-on voltage and \( R_s \) is the series resistance of the diode.

The first equation conveniently decouples the slope efficiency, \( S \), which is a function of both the quantum structure design and the resonator design, the rollover term, which is a function of the thermal properties of the device and the current leakages, and the V-I characteristics of the laser that can be measured. The second equation is valid for well-behaved diode where the V-I characteristic is linear when the diode is forward biased. Neglecting the weak dependence of the rollover term on the driving current, we can differentiate \( \eta_{\text{tot}}(I) \) with respect to current to find the optimal current point,

\[
\frac{d\eta_{\text{tot}}(I)}{dI} = 0 \iff \left[ I^2 - 2 \cdot I_{\text{th}} \cdot I - I_{\text{th}} \cdot V_{\text{turn}} / R_s = 0 \right].
\]

Solving the above quadratic equation for current, we obtain an operating point which gives the maximum electro-optical efficiency

\[
I_{\text{max}} = I_{\text{th}} \cdot \left( 1 + \sqrt{\frac{V_{\text{turn}}}{I_{\text{th}} \cdot R_s}} + 1 \right),
\]

and

\[
\eta_{\text{tot}}^{\text{max}} = \frac{S \cdot Ro}{V_{\text{max}}} \left( 1 - \frac{I_{\text{th}}}{I_{\text{max}}} \right),
\]

where \( V_{\text{max}} = V_{\text{turn}} + R_s I_{\text{max}} \). The optical power, extracted at the peak of the electrical-to-optical efficiency can be expressed as,

\[
P_{\text{opt}}^{\text{max-eff}} = S \cdot Ro \cdot I_{\text{th}} \cdot \sqrt{\frac{V_{\text{turn}}}{I_{\text{th}} R_s}} + 1 \approx \frac{1}{\sqrt{R_s}}, \text{ for } \frac{V_{\text{turn}}}{I_{\text{th}} R_s} \gg 1.
\]

The two most important consequences of the preceding three equations can be stated with respect to the series resistance dependence in the following way:

(A) Smaller series resistance gives maximum efficiency at higher currents and hence allows more power to be extracted

(B) Smaller series resistances give higher absolute values for the maximum electrical-to-optical efficiency (wall-plug efficiency), due to the increase of the \((1-I_{\text{th}}/I_{\text{max}})\) term.

Additionally, \( R_s \) is implicitly present in the rollover term. A smaller series resistance minimizes the rollover at higher currents due to the reduction of contact (Joule) heating which grows as \( R_s I^2 \). For InP-based diodes that have small values for the \( T_0 \) parameter, this is especially important. Eqs. 4-6 should be considered when optimizing the wall-plug efficiency of semiconductor lasers. The threshold current depends on absorption and scattering losses, current leakages, and junction temperature. \( I_{\text{th}} \) has a finite value that scales with the chip size, or more importantly with the junction area. Equation (4) states by how much the maximum (optimum) current can exceed the threshold current,

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\[
\frac{I_{\text{max}}}{I_{\text{th}}} \approx 1 + \sqrt{\frac{V_{\text{turn}}}{I_{\text{th}}^2 R_s}} \approx \frac{1}{\sqrt{R_s}}.
\]

(7)

For high power diode lasers (HPDLs) in the sub-watt power range \(V_{\text{turn}}/I_{\text{th}}\times R_s\) is much greater than unity. Using typical values for HPDL in the 1.55 \(\mu\)m window, and considering 1 mm-long and 100um-emitter wide laser, \(V_{\text{turn}}=0.82\) V, \(I_{\text{th}}=400\) mA, and \(R_s\sim 0.1-0.15\) \(\Omega\), we obtain \(I_{\text{max}}/I_{\text{th}}\sim 4-5\). In section 5, we describe in detail the experiments done to reduce the resistance of the devices.

The above formulation describes the importance of reducing the series resistance of semiconductor lasers in order to increase the wall-plug efficiency. However, it does not describe the thermal behavior of the lasers as the rollover terms are wrapped in the factor \(R_0(I)\). One way to understand the thermal behavior is to self-consistently solve the laser rate equations along with thermal modeling and optical waveguide modeling. However, this is complicated as the simulation domains for the three different properties are varied [3]. While the rate equations need to be solved over the active region and optical mode within the confinement of the photons, the thermal simulation needs to be conducted over a large area including the laser chip and the submounts. While some commercial software e.g. Crosslight have achieved this in a limited scope, it takes a long time to compute the results and it is difficult to match them with the experimental data. We overcame this problem by decoupling the three calculations and solving for the thermal properties using a commercial finite element software package called ANSYS. In a first step the optical mode and confinement factors are calculated using a beam propagation method. Then, the gain and LI properties are calculated using the well-known k.p matrix method, neglecting thermal effects. The thermal effects are then included into the laser characteristics using an empirical model. Since, the above three mentioned methods are well known and documented; we do not dwell on them in this paper but concentrate on the description of the empirical model.

The gain coefficient of the quantum wells is calculated using the k.p matrix [4]. Further the confinement factor of the optical mode is calculated using the beam propagation method. The confinement factor in the cladding layers is also calculated and the internal loss is estimated using various absorption terms like intervalence band absorption, free carrier absorption etc. Based on this, the transparency current (where the modal gain equals internal loss) is estimated. The threshold current and slope efficiency are then calculated using Equations 8 and 9 assuming a logarithmic gain relationship with carrier density (a reasonable assumption for a quantum well active region):

\[
I_{\text{th}} = J_{tr} \cdot w \cdot L \cdot \exp\left(\frac{\alpha_{\text{int}} + \alpha_{\text{mir}}}{\Gamma g_0}\right)
\]

(8)

\[
S = \eta_i \times \frac{1.24}{E_g} \times \frac{\alpha_{\text{int}} + \alpha_{\text{mir}}}{(1 - R_1) + \frac{R_1}{\sqrt{R_2}} \times (1 - R_2)}
\]

(9)

where \(J_{tr}\) is the transparency current density, \(w\) is the width of laser, \(L\) is the length, \(\eta_i\) is the internal quantum efficiency, \(E_g\) is the band gap energy in \(\mu\)m, \(\alpha_{\text{int}}\) is the internal loss, \(\alpha_{\text{mir}}\) is the mirror loss given by expression \((1/L)\ln(1/(R_1\times R_2))\), \(R_1\) and \(R_2\) are the facet reflectivity for optical power for the front and back facet respectively. Using the \(I_{\text{th}}\) and \(S\) values, the light versus current (LI) characteristics can be plotted in the absence of heat dissipation.

In the next step, the thermal heat dissipation and the thermal resistance are calculated using a finite element program like ANSYS [5]. An example of this is shown in Figure 1 for a laser mounted p-side down on a SiC and a diamond heatsink. This helps in understanding how much will the temperature of the active region rise when heat is being generated. Similarly, the series resistance of the device is calculated using the known doping profiles. For a SiC submount and a rise of temperature of \((38.7 – 25)\ C = 13.7\ C\) in the active region, a thermal impedance of 27.4 C/W is extracted for a 750 \(\mu\)m long device mounted p-side down. Only a 2-D calculation was done as the length of the device is much larger than the transverse direction. The thermal impedance varies as \(1/L\) and decreases as the device length is increased.
The CW LI characteristics are then calculated in an iterative manner while using the measured values of $T_0$ (change of threshold with temperature) and $T_1$ (change of slope with temperature). The logic of the calculation is explained in Figure 2. Pulsed LI curves with no heat generation in the active region are plotted for different heat sink temperatures after calculating the change of threshold and slope. A CW curve at normal heat sink temperature is also plotted. Assuming that the degradation of the CW curve is only due to an increase in temperature, then at the intersection of the two curves, the temperature of the active region for the CW case should be equal to the pulsed temperature. Using this logic, the CW curve can be calculated by estimating the power dissipated at a particular current and calculating the temperature for the active region using the simulated thermal resistance. The first iteration assumed that the heat generated in the active region is equal to the total electric power dissipated (given by the multiplication of the voltage across diode calculated using the series resistance and the diode turn-on voltage and the current) less the optical power in the pulsed mode. At a particular current $I$, the threshold and slope for the corresponding pulsed curve (which has the same active region temperature as the CW curve for that current) is calculated using Equations 10 and 11 respectively.

Figure 1. Example of ANSYS thermal simulation with 0.5W of heat dissipated in a 2.5μm wide and 750μm long narrow stripe laser chip ($\approx 3$ degree difference between SiC and Diamond submounts with 0.5W electrical power input).
where $P(I)$ is the power dissipated at that current, and $R_{th}$ is the simulated thermal resistance. From these calculations, the CW optical power is simply calculated using Equation 12.

\[
I_{th}(I) = I_{th} \exp \left( \frac{P(I) \cdot R_{th}}{T_0} \right)
\]  

(10)

\[
S(I) = S \exp \left( \frac{-P(I) \cdot R_{th}}{T_1} \right)
\]  

(11)

In this iteration, we had subtracted the pulsed power (with no heat) from the total electrical power. However, the optical power after the calculation is dropped due to thermal effects. Hence, further iterations are done by subtracting the calculated optical power calculated in the previous iteration from the total electrical power. This is done till the change in the optical power between consecutive iterations is less than the desired accuracy.

\[
L(I) = (I - I_{th}(I)) \cdot S(I)
\]  

(12)

Figure 2. Schematic of using pulsed simulated data to calculate the CW curves under thermal stress.

Figure 3. LI characteristics for a 2 mm long laser when there is no thermal heating, when only T0 parameter is considered, and when both T0 and T1 parameters are considered.
Figure 3 shows the LI characteristics of a 2 mm long laser in the presence of heat dissipation, when only $T_0$ is considered and when both $T_0$ and $T_1$ are considered. It is clear from this figure that for high power lasers, it is not only important to increase $T_0$, but it is also important to increase the $T_1$ value. The $T_1$ parameter depends on both the vertical leakage of carriers by thermionic emission out of the active region leading to reduced internal efficiency and on the increase in internal loss with temperature. In section 6, we describe experiments to improve the carrier confinement in the active region.

Figure 4 shows the calculated LI characteristics for lasers of different lengths for the same epitaxial wafer. The active region consists of 3 QWs in a separate confinement heterostructure. The internal loss $\alpha_{int}$ was calculated to be 6 cm$^{-1}$. The confinement factor $\Gamma$ was 3.24 % and for 1 mm long device mounted p-side down, the thermal resistance was calculated to be 20 K/W and the series resistance was 1.0 $\Omega$. The value for $T_0$ and $T_1$ were 61 K and 106 K respectively. The thermal impedance and the series resistance were assumed to vary as $1/L$ for different length devices. Also plotted is the experimental measurement for a 1 mm long device. There is a very good agreement between the theoretical and experimental values. The model also shows thermal rollover and eventual shutdown of the laser due to thermal effects. The model though simple is very effective in understanding the characteristics of high power lasers. For example in Figure 5 we show the maximum power that can be achieved out of the 1 mm long laser when the thermal resistance is reduced from 50 K/W to 15 K/W.

### 3. EMPIRICAL MODEL FOR SEMICONDUCTOR OPTICAL AMPLIFIERS AND SUPERLUMINESCENT DIODES

An empirical model for calculating the gain of SOAs and the output power for SLDs was constructed similarly. The operating condition for these devices is different since the carriers are not clamped at threshold. Also there are saturation effects that reduce the gain at high output power.

In the first step the optical gain is calculated from the parameters described previously and is given by Equation 13.

$$G_p(I) = \exp\left[\Gamma g_0 * \ln\left(\frac{J(I)}{J_{th}}\right)\right]$$

(13)

It was experimentally observed that since the carriers are not clamped in SLDs and SOAs, there was vertical carrier leakage out of the active region due to thermionic emission as the devices were pumped with higher current. This lead to a reduction in the internal quantum efficiency and a roll-over of the LI characteristics even in very short, low duty cycle pulsed regime. This effect was included in the model by
multiplying the current dependent internal quantum efficiency with the current density in Eqn. 13 above. A way to improve this reduction is further described in section 5.

The amplified spontaneous emission was then calculated using Eqn. 14.

\[
P_{ase} = \frac{hc}{\lambda} * n_{sp} * \Delta \nu * (G_p(I) - 1)
\]

where \(n_{sp}\) is the spontaneous emission factor and \(\Delta \nu\) is the bandwidth of the device.

Thermal effects are then added by assuming that the transparency current density for the pulsed mode at higher temperatures is degraded by \(T_0\) according to Eqn. 15.

\[
J_{tr}(I) = J_{tr} * \exp\left(\frac{P(I) * R_{th}}{T_0}\right)
\]

Gain and ASE are recalculated with the transparency value. Further self-saturation effects are added by reducing the gain due to \(P_{ase}\) with respect to the saturation power. The gain coefficient \(g\) is expressed

\[
g = \frac{g_0}{1 + \frac{P_{ase}}{P_s(I)}}
\]

where \(P_s(I)\) is the saturation power which depends on the current [13]. It is inversely proportional to the carrier lifetime. At high current, Auger recombination significantly affects the carrier lifetime and must be included. The current dependence of the saturation power is therefore included in the model. The calculations are done iteratively till the values for gain and ASE converge to the required accuracy.

Figure 6 shows the calculated ASE power in CW mode for a p-side up mounted 1.5 mm long SLD with 4 QWs. The thermal resistance was measured to be 26 K/W and the series resistance was 0.7 \(\Omega\) for this device. The experimentally measured data is also shown and is in good agreement.

![Figure 6. Simulated and measured LI characteristics for a 1.5 mm long SLD](image)

**4. MEASUREMENT OF THERMAL RESISTANCE**

The importance of reducing thermal resistance in order to increase the output power is seen in Figure 6. The preferred way of reducing the thermal resistance is to mount the semiconductor device p-side down on a heatsink. This way the heat needs to be extracted through only a few microns of semiconductor as opposed to 100 microns of semiconductor when mounted p-side up. Further thicker metal may be used to spread the heat. We have achieved a thermal resistance of ~ 30 K/W for devices mounted p-side up for 1mm long device with 3 \(\mu m\) ridge widths. The thermal resistance for the same device mounted p-side down was ~ 16 K/W.
It is also important to be able to measure the thermal resistance accurately. For semiconductor lasers, the thermal resistance is measured using the Paoli method which relies on the shift of the Fabry-Perot modes as the current is increased and comparing it with the shift due to an increase in temperature [6,12]. However, the Paoli method is not easily applicable to SOAs and SLDs as the Fabry-Perot modes are suppressed to prevent self-oscillations. Also there can be some heating associated even in the pulsed mode which is difficult to extract in the Paoli method. Hence, a new method for measuring the thermal resistance was developed by measuring the LI characteristics in CW operations and comparing it with pulsed measurements with varying heat sink temperature [11]. An example is shown in Figure 7 using a 1.4 mm SLD device with 4 μm waveguide width. For the pulsed operation, the repetition rate was 1 kHz with a pulse width of 4 μs. The CW curve at lower heat sink temperature intersects the pulsed L-I curves at higher heat sink temperatures. If the light output depends only on the active region temperature and the currents, the active region temperature is the same both for the pulse and CW operation at the crossing points. A linear relationship can be defined between the temperature rise of the active region and the heat generation rate using the thermal resistance $R_{th}$ and is defined as:

$$ (T_{a,CW} - T_{h,CW}) = R_{th,CW}P_{CW} \text{ and } (T_{a,pulse} - T_{h,pulse}) = R_{th,pulse}P_{pulse} $$

where $T_a$, $T_h$ are the active region temperature and heat sink temperature respectively, $P$ is the heat generation in the active region and is obtained by subtracting the output optical power from the electrical pumped power. At the point of intersection of two curves, $T_{a,CW} = T_{a,pulse}$, $P_{CW} = P_{pulse} = P$ and hence $T_{h,pulse} - T_{h,CW} = (R_{th,CW} - R_{th,pulse})P$. The value of $T_{h,pulse} - T_{h,CW}$ is plotted versus heat generation in Fig. 8. A linear regression line fits well the experimental data, therefore validating the linear assumption describing the rise of temperature in the active region and the heat generation rate. The slope of the curve in Figure 8 gives the value of $R_{th,CW} - R_{th,pulse}$. For the device plotted in Figure 7, the thermal resistance difference measured was 6 K/W. We further used ANSYS software to calculate the thermal resistance of the device mounted on a copper heatsink. The calculated thermal resistance $R_{th,CW}$ was approximately 18 K/W. For pulsed operation, a transient thermal analysis was done and the heat generation in the active region with pulse width is shown in Figure 9. This behavior was also seen experimentally by a decrease in power in the time interval of the current pulse, as shown in Figure 10. Considering that the L-I curves were measured at 3 μs, the thermal resistance for the pulse was about 8.5 K/W leading to the simulated value of $R_{th,CW} - R_{th,pulse}$ to be 9.5 C/W, close to the experimental value.
It was also observed that the pulsed behavior depended on the value of the series resistance of the device. For the above mentioned experiment, the device had a series resistance of $3 \, \Omega$. It was observed that the heating during the pulse operation reduced when the series resistance was reduced to less than $1 \, \Omega$. The power in the pulse condition started decaying at $\sim 2 \, \mu s$ and was equal to the CW value at $50 \, \mu s$ as opposed to the above mentioned device where the decay started at $1 \, \mu s$ and the pulse power was equal to the CW value within the first $10 \, \mu s$ of the pulse. Hence, it is very important to reduce the series resistance of the device. We describe experiments conducted to achieve this in the next section.

5. REDUCTION OF SERIES RESISTANCE

As seen in Section 2, it is important to reduce the series resistance of the semiconductor devices in order to reduce the thermal load and achieve higher power. The resistance can be decreased by using higher doping concentrations in the cladding regions. However, this decrease in resistance should not be accompanied by an increase in internal loss due to free carrier absorption. Since, the free-carrier absorption is a magnitude higher for the p-dopants as opposed to the n-dopants, various experiments were carried out to study the effect of the p-side doping concentration.

In the first experiment, the dependence of the LI characteristics of broad-area lasers (BAL) with different doping profiles for a two-step SCH configuration was studied. The laser structures used a broadened waveguide with a $1.55 \, \mu m$ InGaAs–InP MQW active region and extremely thick InGaAsP two-step SCH layers [7]. The epitaxial layer structures were grown by chemical beam epitaxy. The p- and n-dopants were Be and Si, respectively. Figure 11 shows a schematic band structure (a) and the doping profiles (b) of different broad-area lasers. The MQW active region consists of four periods of 3-nm thick 0.5% compressively strained InGaAs wells and 20-nm lattice matched InGaAsP ($1.25 \, \mu m$) barriers. The stack of QW/barrier was sandwiched between a 20-nm-thick inner InGaAsP ($1.25 \, \mu m$) bounding SCH layer. The outer InGaAsP ($1.1 \, \mu m$) confining SCH layers were inserted between the p- or n-doped InP cladding layers and the inner SCH layers. Both the bounding and confining layers of the two-step SCH structure were lattice matched to InP. The thickness of the outer InGaAsP confining the SCH layers was $0.7 \, \mu m$, and was intentionally designed to investigate the effect of a two-step SCH layer and the variation of the doping profile. The transverse spot-size in these structures was about $1.6 \, \mu m$ (diameter), larger than in typical laser structures. It has previously been reported that such a large transverse mode is appropriate for high-power semiconductor lasers [8] and leads to better coupling efficiencies to single-mode fibers [9]. Three structures with different doping profiles [as shown in Fig. 11(b)] were tested. The first structure (Type 1) had an undoped two-step SCH layer and a moderately doped p-InP cladding layer with a doping level of $3 \times 10^{17} \, \text{cm}^{-3}$. In the second structure (Type 2), the doping profile of the p-InP cladding layer was graded linearly from $5 \times 10^{16} \, \text{cm}^{-3}$ to $1 \times 10^{18} \, \text{cm}^{-3}$ but the two-step SCH layer was undoped. This structure is similar to more conventional BAL structures used for low internal loss and high output power [8]. For the third structure (Type 3), additional -doped layers were added at the p-InP/1.1 $\mu m$ Q and the 1.1 $\mu m$ Q/1.25 $\mu m$
Q interfaces using a Be $- 2 \times 10^{18}$ cm$^{-3}$ concentration. The outer 1.1 $\mu$m Q confining SCH layer was moderately doped with Be to $1 \times 10^{17}$ cm$^{-3}$. Broad-area lasers with a 100 $\mu$m aperture and 1 mm length were fabricated by using conventional photolithography and metallization.

The measured optical power per facet versus the injected current in the BAL’s at two different temperatures are presented in Fig. 12 for Types 1, 2, and 3 lasers. It is noted that there are significant variations of optical output power depending on the p-doping profiles. For Type 1 and Type 2 lasers, there is little difference in the threshold current, the quantum efficiency and the rolloff power at room temperature, as can be seen from the curves (1) and (2) in Fig. 12. The lower rolloff output power of Type 1 as compared to Type 2 is caused by the higher resistance and the lower electron barrier at the p-InP/1.1 $\mu$m heterojunction due to the lower p-InP cladding doping level in Type 1. However, the slight increase in threshold in Type 2 compared to Type 1 is due to an increase of the free carrier absorption in the higher doped cladding. The curve (3) at 20 C in Fig. 12 clearly shows a dramatic increase of the optical power at high current. The optical power increased almost linearly up to 1.1 W per facet (about four times higher than those of other types). The slope efficiency also increased from 0.13 to 0.19 W/A, and the threshold current is slightly reduced. This improvement is not only due to a reduction in the resistance but also due to less carrier leakage as the doped interfaces provide a barrier for electrons. Similar characteristics were also observed at a high temperature of 45 C as shown in curves (4), (5), and (6) of Fig. 12. The thermal degradation of Type 3 is not severe, although a slight power roll-off appeared at a high injection current of 6 A, corresponding to a current density of 6 kA/cm$.^2$. It is noted that Type 1 shows more thermal sensitivity than Type 2 at high temperature. This is due to an increased thermal load due to higher resistance.

The temperature dependence of the characteristic temperature $T_0$ for the three types of lasers were measured in the range of 20 to 45 C and is shown in Figure 13. It is noted that, in the case of Type 3, the characteristic temperature is very slowly changing within the measurement temperature range, while the
The characteristic temperature of Type 1 and 2 lasers is rapidly decreasing with an increase of the temperature. We note that the characteristic temperature of Type 3 laser is not higher than for the other types of lasers for temperatures around 20 C. This means that the device with a highly doped heterointerface is more immune to thermal degradation at high temperatures in comparison with devices that have undoped heterointerfaces.

In another experiment the grading of the doping profile in the cladding was optimized to reduce the resistance further while maintaining a low value of internal loss. Since, the optical mode decays exponentially in the cladding region, the doping concentration was also profiled with an exponential variation from a value of $3 \times 10^{17}$ cm$^{-3}$ at the InP/1.1 Q SCH to $1 \times 10^{19}$ cm$^{-3}$ at the InP/cap layer. An exponential grading of Be dopants is easy to do in solid source MBE since it translates to a linear ramp of temperature. A series resistance of 0.5 $\Omega$ was achieved for a 1 mm long device with 3.0 $\mu$m wide ridge. The internal loss was kept below 6 cm$^{-1}$.

### 6. CARRIER CONFINEMENT LAYERS

While using multiple quantum wells, there is an inherent bandwidth-power relationship as shown in Figure 14 where the power and bandwidth of published results and commercial devices is plotted. If one increases the power by changing the number of QW’s, then the bandwidth decrease sharply. It is thus, important to increase the efficiency of the SLED devices. In the InGaAsP/InP system used in 1.55 $\mu$m wavelength region, the conduction band offset between InP and the active material is small. This leads to thermionic emission of electrons out of the active layer causing the internal quantum efficiency to drop. For high injection SOAs and SLDs, it is important to keep the vertical leakage of the carriers especially the electrons, out of the active region low. Vertical leakage reduces the internal quantum efficiency as the value of injected current is increased. This is especially acute for SOAs and SLDs as opposed to lasers where the Fermi energy level is clamped. Carrier stopper layers at the intersection of InGaAsP separate confinement heterostructure (SCH) and p-doped InP were investigated [10]. Three wafers were grown by solid-source MBE. The active region consisted of InGaAsP multi-quantum wells in a thin separate confinement heterostructure (SCH). A standard wafer was grown with no electron stopper layer. This wafer had a doping spike at the InP-SCH to reduce the thermionic emission. Two wafers were grown with electron stopper layer

![Figure 13. Characteristic temperature for different doping profiles.](image)
between the InP cladding and the SCH as is shown in Fig. 15. One wafer had the electron stopper layer p-doped to $8 \times 10^{17} \text{cm}^{-3}$, whereas in the other, the electron-stopper layer was undoped. The series resistance of the device was optimised to reduce the heat load on the device and prevent thermal rollover. A 3.2 mm ridge semiconductor angled stripe was processed using standard lithography and metallization techniques. The waveguide width and etch depth were optimised to reduce the facet reflectivity. The waveguide width was also optimised for high power and coupling to a single mode fiber. The SLED chips were cleaved at a length of 1.5 mm and mounted p-side up on a ceramic sub-mount cooled by a thermo-electric cooler (TEC). The waveguide ridge was angled at 8° and each facet was anti-reflection (AR) coated to less than $10^{-3}$, leading to an effective facet reflectivity of less than $1 \times 10^{-5}$.

Ten devices from each of the wafer were measured for their light-versus current (LI) characteristics in CW mode. Currents up to 1 A were applied and output power measured by an integrating sphere. The submounts were cooled to 25°C for all the measurements. Figure 15 shows the summary of the maximum power achieved in devices from the three wafers. Average power along with the minimum and maximum power for each type of SLED devices is plotted. The average power for devices with no electron stopper

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**Fig. 14.** Relation between power and bandwidth for 1550 nm SLEDs

**Fig. 15.** Maximum power for devices for different wafers

**Fig. 16.** LI characteristics for devices with and without electron stopper (ES)

**Fig. 17.** 3-dB bandwidth with current for devices with and without electron stopper layer
layer is 9.9 mW compared to 12.3 mW for device with undoped electron stopper, and 15.2 mW for devices with doped electron stopper layer. This corresponds to an increase of 1.8 dB in power. A similar increase is observed if only the best devices are considered for the three different cases.

The best of the devices from the wafers without electron stopper layer, and with doped electron stopper layer were further mounted on copper heatsinks and remeasured for the LI characteristics in CW mode. The LI characteristics are shown in Figure 16. The chip on submount measurements are also plotted for comparison. We see an increase in the total power for both cases due to better heatsinking. A maximum power of 33 mW is achieved at a current of 720 mA for the devices with doped electron stopper layer. For the device without the electron stopper layer, a maximum power of only 19 mW is achieved at a current of 660 mA. This corresponds to an increase in power by 2.2 dB. It is also observed that the SLDs with electron stopper layer start rolling over at a higher current that the devices with no electron stopper layer. The reason for the difference is not thermal but lower degradation of internal quantum efficiency due to vertical carrier leakage. The 3-dB bandwidth of the spectrum of the device on heatsink was also measured and is plotted for devices with and without electron-stopper layer in Figure 17. A maximum bandwidth of 98 nm is achieved for both kind of devices at a current of 1 A. The bandwidth increases linearly with current showing the true ASE source nature. At the current where maximum power is achieved (720 mA for device with electron stopper, and 660 mA for the device without electron stopper), a 3-dB bandwidth of greater than 80 nm is achieved. This shows that we have increased the power in the SLED without decreasing the bandwidth. This is important to move out of the bandwidth-power curve.

7. CONCLUSION

In conclusion, we have demonstrated an empirical model to characterize the performance of high power lasers, semiconductor optical amplifiers and super-luminescent diodes in thermal stress conditions. We have shown that by using a simplified model, the LI characteristic of these devices can be predicted accurately. Further, parameters like thermal resistance, series resistance, and internal quantum efficiency were identified for high performance. A method was presented to measure the thermal resistance by comparing the CW LI characteristics with the pulsed values. Further it was found that there can be appreciable heating during a pulse which needs to be characterized. Methods to decrease the thermal resistance were experimentally verified leading to an appreciable increase in optical power. Finally, carrier stopper layers were investigated and found to maintain the internal quantum efficiency in SLDs leading to an increased optical power.

REFERENCES