PhD Qualifier Exam, Spring 2017

Computer Architecture and Systems

1. (8 points) Short Answer Questions.
(a) (2 points) What is *virtual memory*? Give two reasons for implementing virtual memory in a computer system.

(b) (3 points) Explain how a software-managed TLB (translation lookaside buffer) differs from a hardware-managed TLB. What are the advantages and disadvantages of using a software-managed TLB?

(c) (3 points) What is a *stack frame* (also called *activation record*)? Explain how *stack frames* are used for implementing *functions* (also called *subroutines*) in assembly language programs.

2. (5 points) A single-cycle unpipelined processor has a clock cycle of 50 ns. An 8-stage pipelined version of the same processor is built as follows:

(i) Fetch stage 1 : 7 ns
(ii) Fetch stage 2 : 8 ns
(iii) Decode/Register read stage : 5 ns
(iv) ALU stage 1: 7 ns
(v) ALU stage 2: 7 ns
(vi) Memory access stage 1 : 7 ns
(vii) Memory access stage 2 : 8 ns
(viii) Writeback/End stage : 4 ns

Each pipeline latch has a latency of 1 ns.

(a) (2 points) Calculate the maximum clock speed possible for this pipelined processor.

(b) (3 points) What is the best case speedup possible with this pipeline over the unpipelined implementation? Assume that there are no control hazards and data hazards.

3. (7 points) Consider a *video streaming* workload that accesses a 512 KB data sequentially, 4 bytes at a time, with the following address stream: 0, 4, 8, 12, 16, ...

(a) (1 point) What type of locality should a cache memory system exploit for obtaining good performance with such type of workload? Why?

(b) (2 points) A computer system has a 32 KB direct-mapped cache with 32-byte blocks. Determine the miss rate experienced by this cache memory for the workload described above.

(c) (4 points) State two techniques that can be used to improve the cache memory performance for such a workload. Explain why these two techniques give good performance.