PhD Qualifier Exam, Fall 2018

Computer Architecture and Systems

1. (8 points) Short Answer Questions.
(a) (2 points) Explain why *miss rate* is not a good metric for evaluating cache memory performance.

The average access time in a cache memory system is given by:

$$T_{avg} = T_{hit} + mT_{miss}$$

A cache memory may have low miss rate (m), but a high access time (T_{hit}), making it have lower performance than one with a higher miss rate.

(b) (2 points) Explain how hardware interrupts are utilized in implementing multitasking and process management.

For implementing multitasking, there has to be provision for stopping a user program (after it has run a quantum of time) so that the operating system can take control. In systems that implement multitasking, a hardware timer periodically sends hardware interrupts to the processor.

(c) (2 points) Explain the disadvantages of using a single-cycle datapath in a CPU implementation. Give at least two reasons.

1. With a single-cycle datapath, the clock cycle must be very long so as to accommodate the instruction that requires the longest execution time.
2. With a single-cycle datapath, it is not possible to pipeline the execution of instructions.

(d) (2 points) Explain how an assembly language program can pass parameters to a function (aka subroutine). Mention at least two methods.

Parameters can be passed to a function through (i) registers, (ii) stack, or (iii) both. Passing parameters through registers is the most efficient; however, only a small number of parameters can be passed in this manner.

2. (6 points) Processors P1 and P2 implement two different instruction set architectures (ISAs). P1 runs at a clock rate of 2.5 GHz and P2 runs at 3.0 GHz. Both ISAs have 4 classes of instructions, {A, B, C, D}. The average cycles per instruction (CPI) for these 4 classes of instructions in the two processors are given in the first two rows of the table below. The last two rows of the table give the instruction distribution when an application program was compiled for the two processors. (Both executables have the same dynamic instruction count, but different instruction distributions.) Determine which processor will execute this application program faster. What is the speedup of the faster one over the slower one? Show work to get credit.

	Class A	**Class B**	**Class C**	**Class D**
CPIs in P1	1	2	3	4
CPIs in P2	2	1	4	3
Frequencies in P1	10%	10%	50%	30%
Frequencies in P2	20%	10%	40%	30%

Average CPI for P1 $= 1 \times 0.1 + 2 \times 0.1 + 3 \times 0.5 + 4 \times 0.3 = 3.$
Average CPI for P2 $= 2 \times 0.2 + 1 \times 0.1 + 4 \times 0.4 + 3 \times 0.3 = 3.$
Average instruction execution time for P1 $= \text{CPI} \times \text{CT} = \frac{3}{2.5 \times 10^9}$
Average instruction execution time for P2 $= \text{CPI} \times \text{CT} = \frac{3}{3 \times 10^9}$
P2 is faster than P1, as its execution time is lower.
Speedup $= \frac{\text{Instruction execution time for P1}}{\text{Instruction execution time for P2}} = 1.2.$

3. (6 points) Consider the following two cache configurations. Determine which configuration will result in shorter average memory access time. Show work to get credit.

Parameter	**Configuration 1**	**Configuration 2**
L1 Cache Size	1 MB	256 KB
L2 Cache Size	-	768 KB
L1 Hit Rate	92%	70%
L2 Hit Rate	-	85%
L1 Access Time	4 ns	2 ns
L2 Access Time	-	8 ns
Main Memory Access Time	100 ns	100 ns

Average access time for Configuration 1 = $T_{hit} + mT_{miss}$ = 4ns + $0.08 \times$ 100ns = 12ns
Average access time for Configuration 2 = $T_{hit1} + m1(T_{hit2} + m2 \times T_{miss2})$ = 2ns + 0.3(8ns + $0.15 \times$ 100ns) = 8.9ns
Therefore, Configuration 2 gives shorter average memory access time.