ENEE 759H

Course Overview

This course introduces students to the issues involved in high-speed chip-level interfaces in the context of DRAM systems design. General topics include high-speed signaling mechanisms, signal integrity, synchronization mechanisms, meeting skew budgets, packaging, and power consumption. DRAM-specific topics include studies of modern high-performance DRAMs (DDRx SDRAM, Rambus, RLDRAM) and future designs (Hybrid Memory Cube, Buffer on Board). Students will work in groups on a research-oriented project that may involve simulation, modeling, and/or fabrication of prototype chips.

Course Prerequisite(s)

Ideally, a student will have taken ENEE646 or perhaps ENEE446. Students must have knowledge of digital logic design and computer organization. For example, you should understand digital design concepts such as multiplexers, gates, boolean algebra, finite-state machines, and flip-flops. You should understand fundamental computer organization: what the program counter is, what a register file is for, how busses are used, what happens in the hardware to effect instruction execution, etc. It would help if you also understand and are reasonably fluent in programming Verilog (or C or Perl, because Verilog is very C-like, as is Perl).

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