ENEE750: VLSI Design Automation

Spring, 2014

Course Goals:

Deep nanometer scale (32, 22, 16, 11 nm and beyond) VLSI design calls for innovative techniques for temperature rise reduction within chips and in packages. This fourth optimization criterion together with those of speed, area, and power dissipation, presents new challenges to the EDA (Electronic Design Automation) industry. This course will provide students with knowledge and skills that will enable them to develop commercial quality CAD tools.

The students will learn the essence of theoretical models and techniques to automate the physical design processes of VLSI circuits so as to optimize the above mutually conflicting objective functions. They will then create a proper model for a specific real-world problem, devise proper techniques, and write efficient code. Other present-day topics may include issues on 3D chips, SiP (System in Package), and carbon nanotube interconnects.

Prerequisites:

Basic knowledge of data structures and algorithms (e.g., CMSC 451, ENEE641), and familiarity with a high-level programming language (C/C++).
***ENEE640: Digital VLSI Design is NOT a prerequisite*.**

Texts: (1) N. Sherwani, *Algorithms for VLSI Physical Design Automation*, 3rd Edition, Kluwer Academic Publishers, Boston, MA, 1999, and
(2) lecture notes/papers from current literature.

References: (Recommended, ENEE641 textbook) T. H. Corman, C. E. Leiserson, R. L. Rivest, and C. Stein, *Introduction to Algorithms*, 2nd Edition, McGraw-Hill, Boston, MA, 2001.

Course Topics:

- Overview of VLSI design
- Design and fabrication of VLSI devices
- 3D VLSI chips and System in Package
- Data structures and basic algorithms
- Partitioning
- Floorplanning
- Placement

- Global routing
- Detailed routing
- Multi-level routing
- Thermal analysis
- Deep nanometer scale VLSI design
- Carbon nanotube wires and vias

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