ECE Written Qualifying Examination, Circuits Spring 2019

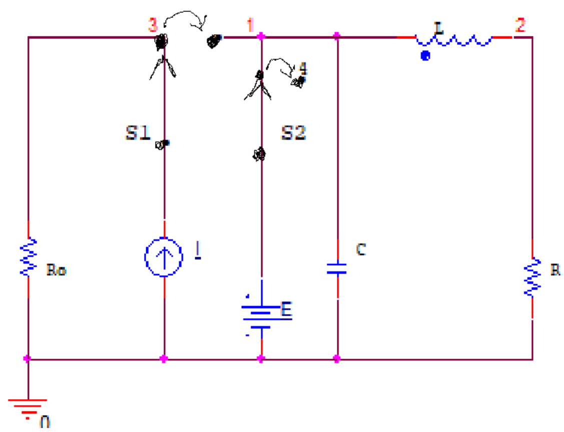
1. 7 points

The following circuit is assumed to have existed for all time. At t=0 the switch S1 switches from node 3 to node 1 (connecting I to the RLC circuit) and S2 opens (switching from node 1 to node 4, thus disconnecting E). I and E are constant, DC, current and voltage, respectively; R, Ro, L and C are positive element values.

a) (3 points) Set up the (second order) differential equation for $v_1(t)$ for t>0 [where v_1 is the capacitor node voltage measured with respect to ground].

b) (3 points) Find the following capacitor voltage and current values immediately before and after switching, $v_1(0-)$, $Cdv_1/dt(0-)$ and $v_1(0+)$, $Cdv_1/dt(0+)$.

c) (1 point) Give the final values $v_1(\infty)$ and inductor current $i_L(\infty)$ [entering the dot].



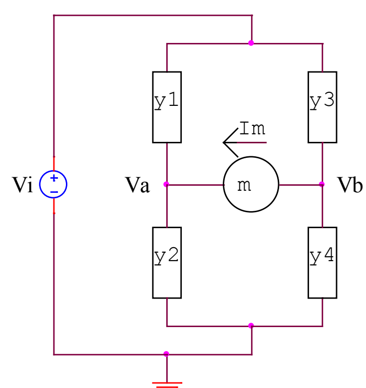
2. 6 points

In the following bridge circuit the meter in the center is an amp-meter with input resistance of 0 Ohms. Vi is the voltage of the voltage source and the four branches are described by their admittances, y_i, i=1, 2,3,4. The current Im in the meter is known to be given by

$$Im = [(y_2 \cdot y_3 - y_1 \cdot y_4)/(y_1+y_2+y_3+y_4)]Vi$$

a) (3 points) Find the relationship between the y_i such that the bridge is in balance, that is when Im=0.

b) (3 points) If y_1 at balance is perturbed to become $y_5=y_1+\Delta y_1$ [where y_1 is as in a)] and y_2 and y_3 are unperturbed, find the perturbation Δy_4 of y_4 such that $y_4+\Delta y_4$ returns the bridge to balance.



3. 7 points

When the following NMOS transistor is in saturation (that is when $V_{DS} \geq V_{GS}$-Vth) its drain current is described by (k and the threshold voltage Vth are both positive)

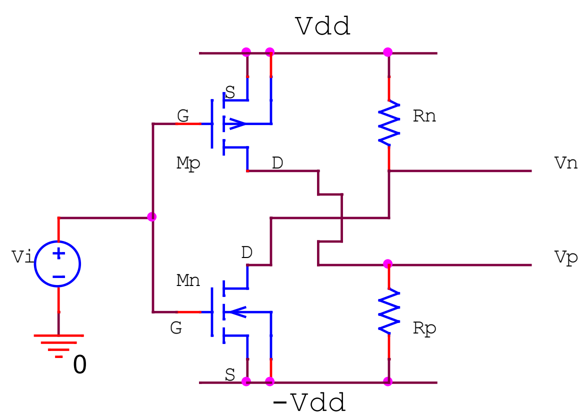
$$I_D = k(V_{GS} - Vth)^2 \qquad \text{[for NMOS]}$$

Assume also that the PMOS is completely complementary, that is (with the same k and Vth) so that

$$I_S = k(V_{SG} - Vth)^2 \qquad \text{[for PMOS]}$$

(here the source current I_S and the drain current I_D are taken as positive when going into the source, S, and the drain, D, respectively)

The bias voltage Vdd is large enough to make the circuit operational [note the presence of the negative bias].



a) (3 points) When the input voltage is zero, Vi=0, find the maximum resistance value, Rn=Rmax [in terms of k, Vth and Vdd], such that the NMOS transistor is in saturation.

b) (3 points) Again at Vi=0 and when Rn and Rp are both smaller than Rmax, find the output difference voltage, Vdiff=Vn-Vp, (again in terms of k, Vth and Vdd) [Vn and Vp are measured with respect to ground].

c) (1 point) Is it possible to design the circuit to obtain Vdiff = 0 when Vi=0? Explain your answer.

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#1. The circuit for $t>0$ is

a) then KCL: $I = i_c + i_L$

$\Rightarrow i_L = I - C\frac{dv_1}{dt}$

KVL: $v_1 = L\frac{di_L}{dt} + Ri_L$ ∴ from KCL $+C\frac{d^2v_1}{dt^2} = 0 - \frac{di_L}{dt} = -\frac{1}{L}(v_1 - Ri_L) = -\frac{1}{L}v_1 + \frac{R}{L}\left(I - C\frac{dv_1}{dt}\right)$ (KVL, KCL)

$\Rightarrow C\frac{d^2v_1}{dt^2} + RC\frac{dv_1}{dt} + \frac{1}{L}v_1 = \frac{RI}{L}$

b) as the original configuration is at a steady DC state at $t=0_-$ ∴ $v_1(0_-) = E$, $C\frac{dv_1}{dt}(0) = i_c(0) = 0$

after the switch change v_1 & i_L can not jump (to avoid impulse)

so $v_1(0_-) = v_1(0_+)$, $i_L(0_-) = E/R = i_L(0_+) \Rightarrow i_c(0_+) = I - i_L(0_+)$

∴ $v_1(0_+) = E$, $C\frac{dv_1}{dt}(0_+) = I - E/R$

c) From the above figure $i_c(\infty) = 0 \Rightarrow i_L(\infty) = I$ & $v_L(\infty) = 0 \Rightarrow v_1(\infty) = R\,i_L(\infty) = RI$

#2. a) at balance $i_M = 0 \Rightarrow y_2 y_3 = y_1 y_4$

b) In the new balance $y_2 y_3 = (y_1 + \Delta y_1)(y_4 + \Delta y_4) = y_1 y_4 + [y_4 \Delta y_1 + y_1 \Delta y_4 + \Delta y_1 \Delta y_4]$

$\Rightarrow [\cdot]$ term $= 0 \Rightarrow 0 = y_4 \Delta y_1 + (y_1 + \Delta y_1)\Delta y_4 \Rightarrow \Delta y_4 = \frac{-\Delta y_1 y_4}{y_1 + \Delta y_1}$

#3. a) $V_{GS_n} = V_{dd}$, $V_{DS_n} = 2V_{dd} - R_n \cdot k(V_{GS_n} - V_{th})^2 \geq V_{GS_n} - V_{th}$

$\Rightarrow 2V_{dd} - R_{n_{max}} \cdot k(V_{dd} - V_{th})^2 = V_{dd} - V_{th}$

$\Rightarrow V_{dd} + V_{th} = R_{n_{max}} \cdot k(V_{dd} - V_{th})^2 \Rightarrow R_{n_{max}} = \frac{V_{dd} + V_{th}}{k(V_{dd} - V_{th})^2} = R_{max} = \frac{1}{k(V_{dd} - V_{th})}$

b) $V_n = V_{dd} - R_n k(V_{dd} - V_{th})^2$, $V_p = R_p \cdot k(V_{dd} - V_{th})^2 + (-V_{dd})$

$\Rightarrow V_n - V_p = V_{dd} - R_n k(V_{dd} - V_{th})^2 - (-V_{dd}) - R_p \cdot k(V_{dd} - V_{th})^2$

$= 2V_{dd} - (R_n + R_p)k(V_{dd} - V_{th})^2 = V_{diff}$

c) We need $V_n - V_p = 0 \Rightarrow (R_n + R_p) \cdot k(V_{dd} - V_{th})^2 = 2V_{dd}$ or $R_n + R_p = \frac{2V_{dd}}{k(V_{dd} - V_{th})^2}$

The maximum $(R_n + R_p)$ can be

is $\max(R_n + R_p) = 2R_{max} = \frac{2V_{dd}}{k(V_{dd} - V_{th})^2} + \frac{2V_{th}}{k(V_{dd} - V_{th})^2}$

as this exceeds by $\frac{2V_{th}}{k(V_{dd} - V_{th})^2}$ the amount needed to force $V_n - V_p = 0$

we can chose $R_0 = R_n = R_p = R_{max} - \frac{V_{th}}{k(V_{dd} - V_{th})^2}$ to make $V_n - V_p = 0$