PhD Qualifier Exam, Spring 2019

Computer Architecture and Systems

1. (6 points) Consider an assembly-level architecture, with its own assembly language. If a new instruction called `exp` is added to this assembly-level architecture, explain in detail the change(s) that should be made (if at all) to:
(a) the compiler (high-level language → assembly language translator)?

(b) the assembler (assembly language → machine language translator)?

(c) the CPU control unit (machine language → microinstruction interpreter)?

2. (8 points)
(a) (3 points) Explain (with a flowchart diagram) how the memory management unit (MMU) translates memory addresses in a paging-based virtual memory system. You can assume that there is no translation lookaside buffer (TLB).

A virtual memory system uses 16-bit virtual addresses. The physical memory consists of 8 Kbytes. The page size is 4 Kbytes. The translation lookaside buffer (TLB) has 3 entries. Both the TLB and the page table are replaced using the LRU (least recently used) policy.

(b) (1 point) Indicate using a diagram how the memory management unit (MMU) would split a 16-bit address to get the virtual page number (VPN).

(c) (2 points) Consider the following sequence of memory address accesses: 0x6ffc, 0x7ffc, 0x6000, 0x4000, 0x3000, 0x2000, 0x7ffc, 0x2008, 0x74fc, 0x64fc. For each of these accesses, indicate if it would be a TLB hit or miss. Also indicate if it would be a page fault or not.

Virtual Addr	VPN	TLB hit/miss	Page Hit/Fault	TLB index	Physical Page
0x6ffc					
0x7ffc					
0x6000					
0x4000					
0x3000					
0x2000					
0x7ffc					
0x2008					
0x74fc					
0x64fc					

(d) (2 points) Draw the final state of the TLB and the page table. That is, show the contents of each entry in the TLB and the page table.

3. (6 points)
(a) (3 points) With the help of a pipeline timing diagram, explain how branch prediction can be used to deal with control hazards in a pipeline.

(b) (3 points) With the help of a pipeline timing diagram, explain how exceptions are handled in program order in a pipeline.