Class Exercise—Logic Design with Decoders and Multiplexers

11/2/15

1. Using or-gates and/or nor-gates along with a 3-to-8 line decoder, realize the following pair of expressions. The gates should be selected so as to minimize their total number of input terminals.

$$f_1(x_2, x_1, x_0) = \sum m(0,2,4)$$
$$f_2(x_2, x_1, x_0) = \sum m(1,2,4,5,7)$$

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2. Realize the Boolean expression

$$f(w, x, y, z) = \sum m(4,5,7,8,10,12,15)$$

using a 4-to-1 line multiplexer and external gates

(a) Let w and x appear on the select lines S_1 and S_0, respectively.

(b) Let y and z appear on the select lines S_1 and S_0, respectively.