## Class Exercise—Logic Design PLAs and PALs

11/4/15


1. The following set of Boolean functions is to be realized with a $3 \times 4 \times 2$ PLA having both true and complemented outputs (see example above). Draw the logic diagram of the realization in PLD notation and show the corresponding PLA table.

$$
\begin{aligned}
& f_{1}(x, y, z)=\sum m(0,4,5,6) \\
& f_{2}(x, y, z)=\sum m(0,1,3,7)
\end{aligned}
$$

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11/4/15


Figure 5.62 A simple four-input, three-output PAL device
2. Using the PAL device pictured above, draw the logic diagram of a realization in PLD notation for the following set of Boolean functions:

$$
\begin{gathered}
f_{1}(x, y, z)=\sum m(1,2,4,6,7) \\
f_{2}(x, y, z)=\sum m(2,4,5,6) \\
f_{3}(x, y, z)=\sum m(1,4,6)
\end{gathered}
$$

