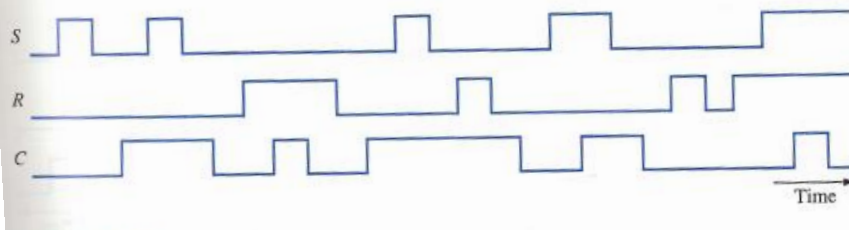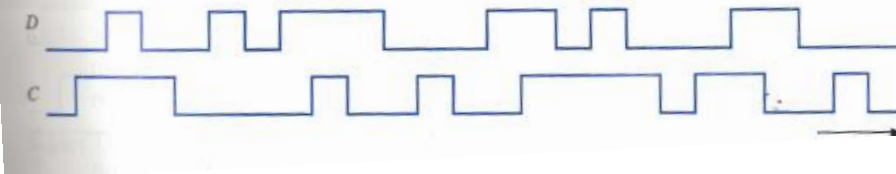# Class Exercise—Latches and Flip-Flops

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6.4 The input signals shown in Fig. P6.4 are applied to the gated SR latch of Fig. 6.5a when initially in its 0-state. Sketch the Q and $\overline{Q}$ output signals. Assume all timing constraints are satisfied.
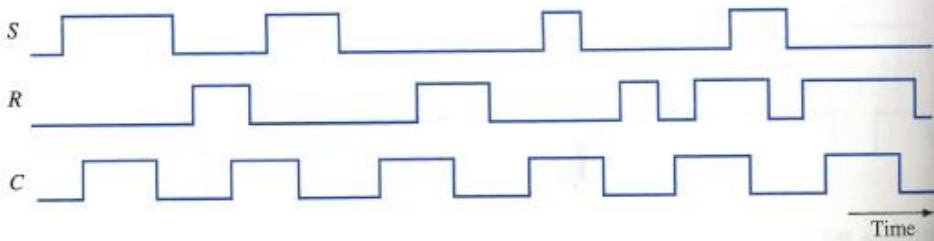

6.5 The input signals shown in Fig. P6.5 are applied to the gated D latch of Fig. 6.6a when initially in its 0-state. Sketch the Q and $\overline{Q}$ output signals. Assume all timing constraints are satisfied.

6.6 The input signals shown in Fig. P6.6 are applied to the master-slave SR flip-flop of Fig. 6.12a when initially in its 0-state. Sketch the Q_M, $\overline{Q}_M$, Q_S, and $\overline{Q}_S$ output signals. Assume all timing constraints are satisfied.

6.7 The input signals shown in Fig. P6.7 are applied to the master-slave JK flip-flop of Fig. 6.14a when initially in its 0-state. Sketch the Q_M and Q_S output signals. Assume all timing constraints are satisfied.