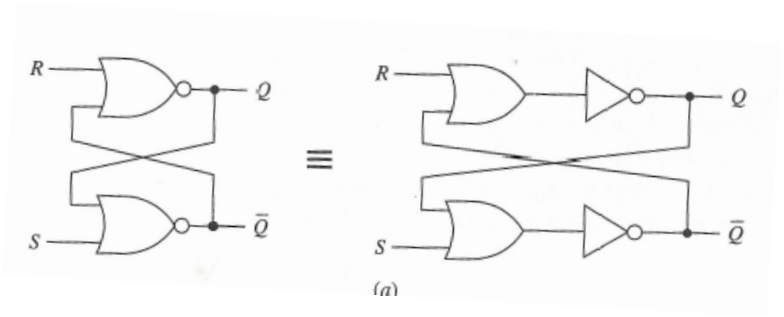
Latches and Flip-Flops
ENEE 244-010x

SR-Latch

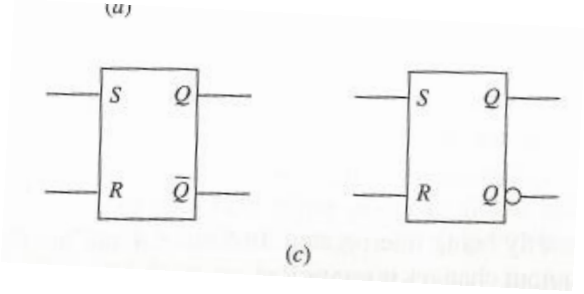


Logic Diagram

Inputs		Outputs	
S	R	Q^+	$\bar{Q}^+$
0	0	Q	$\bar{Q}$
0	1	0	1
1	0	1	0
1	1	0*	0*

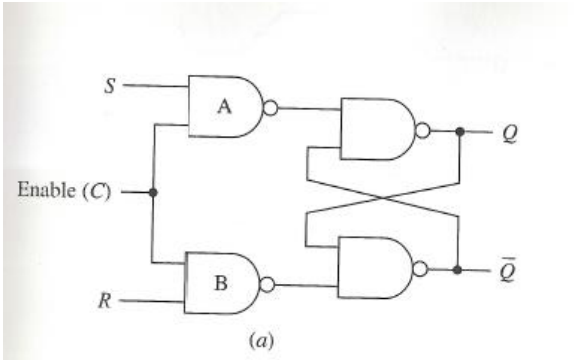
*Unpredictable behavior will result if inputs return to 0 simultaneously

Truth Table



Symbol

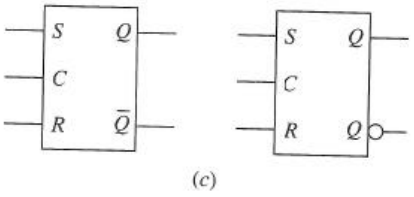
Gated SR-Latch



Inputs			Outputs	
S	R	C	Q^+	$\bar{Q}^+$
0	0	1	Q	$\bar{Q}$
0	1	1	0	1
1	0	1	1	0
1	1	1	1*	1*
X	X	0	Q	$\bar{Q}$

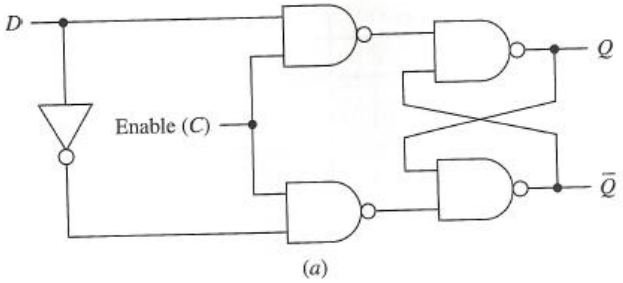
*Unpredictable behavior will result if S and R return to 0 simultaneously or C returns to 0 while S and R are 1

(b)



Decoders, Encoders and Multiplexers
ENEE 244-010x

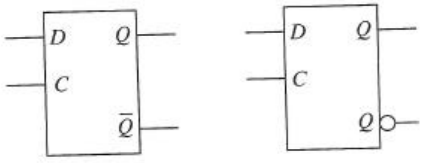
Gated D-Latch



(a)

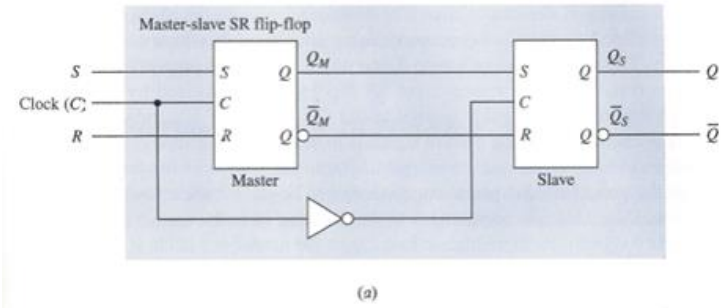
Inputs		Outputs	
D	C	Q^+	$\overline{Q}^+$
0	1	0	1
1	1	1	0
X	0	Q	$\overline{Q}$

(b)



(c)

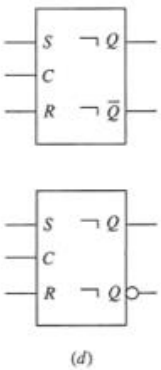
Master-Slave SR Flip-Flop



(a)

Inputs			Outputs	
S	R	C	Q^+	$\overline{Q}^+$
0	0	⊓	Q	$\overline{Q}$
0	1	⊓	0	1
1	0	⊓	1	0
1	1	⊓	Undefined	Undefined
X	X	0	Q	$\overline{Q}$

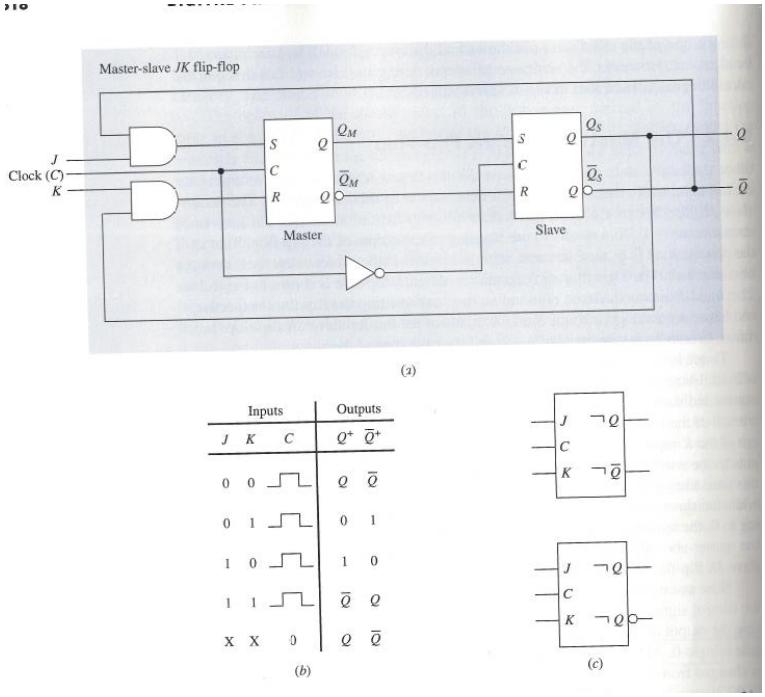
(c)



(d)

Decoders, Encoders and Multiplexers
ENEE 244-010x

Master-Slave JK Flip-Flop



Positive Edge Triggered D Flip-Flop

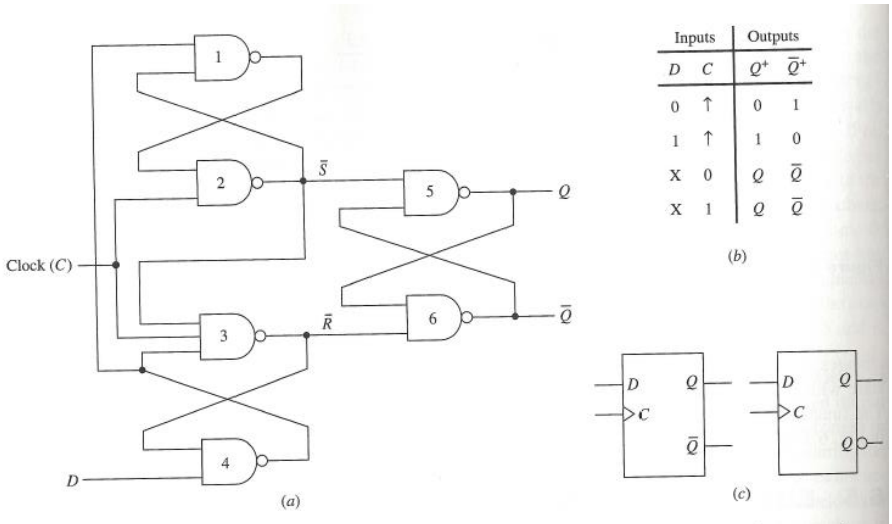


Figure 6.18 Positive-edge-triggered *D* flip-flop. (*a*) Logic diagram.(*b*) Function table where Q^+ denotes the output *Q* in response to the inputs. (*c*) Two logic symbols.

Positive Edge-Triggered T Flip-Flop

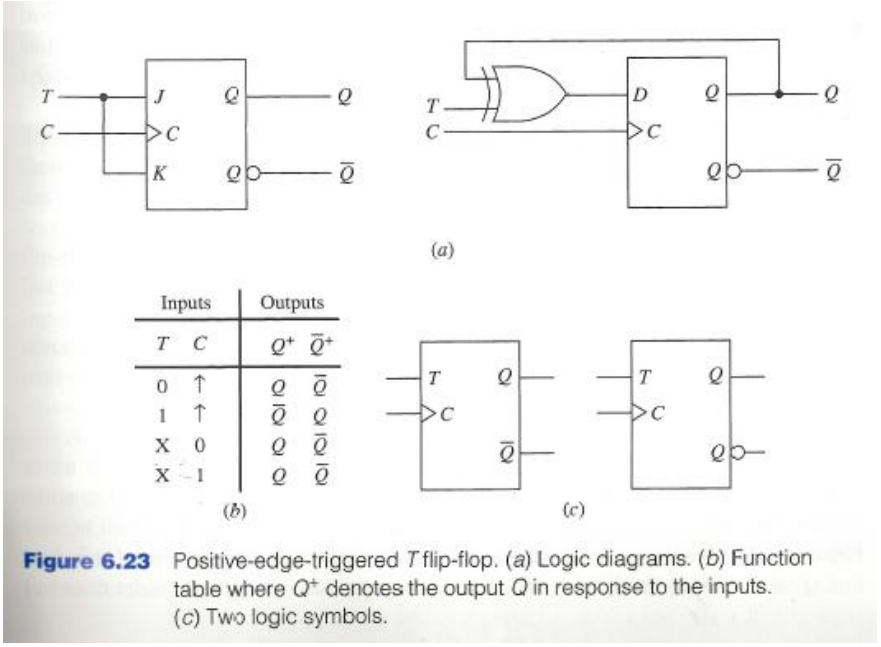


Figure 6.23 Positive-edge-triggered *T* flip-flop. (*a*) Logic diagrams. (*b*) Function table where Q^+ denotes the output Q in response to the inputs. (*c*) Two logic symbols.