Low-Cost Back Contact Silicon Solar Cells
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Abstract—Back-contacted solar cells offer multiple advantages in regard of reducing module assembling costs and avoiding grid shadowing losses. The investigated emitter-wrap-through (EWT) device design has an electrical connection of the front emitter and the rear emitter grid in form of small holes drilled into the crystalline silicon wafer. The thus obtained cell structure is especially suitable for low-cost base material with small minority carrier diffusion lengths. Different industrially applicable solar cell manufacturing processes for EWT devices are described and compared. The latest experimental results are presented and interpreted; especially the photo-current is found to be distinctly increased. The relation between open circuit voltage and rear side passivation is discussed based on two-dimensional (2-D) computer simulations.

Index Terms—Back contact solar cell, commercially applicable process, EWT, low-cost process.

I. INTRODUCTION

 Compared to conventional solar cells back contact devices (i.e., both contacts on the rear) offer multiple advantages, such as the facilitation of the cell interconnection in the module and the avoiding of grid shadowing losses. According to investigations by solar cell manufacturers, module production costs can be cut by half due to the back contact design [1]. In recent years, several research institutions [2]–[6] and solar cell companies [7] were aiming at the further development and optimization of rear-contacted solar cells. Two major approaches were studied: one uses high-quality silicon base material with high-minority carrier diffusion lengths and collecting junctions only at the rear side. Thus, the charge carriers which are generated near the front side have to travel through the whole cell volume to be collected. The highest so far reported efficiency was 26.8% on a 1.56-cm² point contact concentrator (50 suns) solar cell [8] applying cost intensive manufacturing techniques such as aligned photolithography and high-temperature oxidations. The emitter wrap-through (EWT) cell as second design type is equipped with two carrier collection junctions (on front and rear surfaces). Both surfaces are electrically connected through conducting paths in the form of holes [2], [3], [9] which allows them to use silicon with diffusion lengths smaller than the device thickness (e.g., multicrystalline silicon) appropriate for cost reasons. Additionally, the collection efficiency of photogenerated carriers in the bulk is distinctly increased by the double junction. Low-cost EWT solar cells reached efficiencies of 12.2% with a single ARC.

In the following, a manufacturing process of EWT solar cells is presented which fully relies on low-cost steps. Two different methods were studied for high throughput hole formation. To optimize the critical definition of the interdigitated p/n-area at the cell rear side, several techniques were investigated. Interdigitated finger grids are used for base and emitter contacts. Metallization is carried out by screen printing, which is a reliable technique in industrial practice. In order to detect the crucial process steps and to facilitate the optimization of the cell design, computer simulations have been carried out.

II. THE EWT DESIGN

Fig. 1 presents a schematic illustration of our EWT cell design (rear side). Both contacts (emitter and base contact) are located at the cell rear which considerably facilitates the connection of the solar cells to modules. Series connection of standard solar cells is typically performed by soldering metal tapes from front to rear side of neighboring cells which is difficult to automate for a high-volume cell production. For back contact devices, the terminals to be connected are on the same side. Front and rear emitter are electrically connected (wrapped) through macroscopic holes in the wafer. A rear emitter is necessary as contact area but also desirable to improve the internal collection efficiency. One of the big advantages of an EWT—compared to a conventional cell—is the grid-free front side which induces a distinctly enhanced short-circuit current. Another advantage is the appealing uniform appearance which may find an increasing interest for solar modules in façades.
Fig. 2. SEM picture of an EWT cell rear side. In the middle, a connecting hole is shown. On the left, an emitter metal contact is shown. The deepening after milling of the n$^+$-doped layer (on the right) enables the contacting of the base.

III. TECHNOLOGY

The most particular point in an EWT-cell process is the connection of the front emitter and the rear n-type grid. Numerous holes (40–100 holes/cm$^2$) through the wafer are required in order to obtain reasonable series resistances. In this study, two different methods were studied for hole formation: a wafer dicing saw was used to create the holes by perpendicular overlapping cuts into the wafer front and rear side. For experimental studies, a single blade with rectangular cross section and 150-$\mu$m blade-width was used; for industrial production, a structuring wheel or multi-blade tool would be more suitable. With the latter two methods, a throughput of one wafer/h is intended [10]. Alternatively, holes were drilled by laser, which is a very flexible technique for experimental studies. Depending on the required hole density, the mechanical method has by a factor of up to five higher throughput than the fastest Q-switched lasers on the market as a study of Gee et al. indicated [2].

The second crucial point in a back contact cell process is the definition of the p/n-region at the cell rear. Renouncing on expensive photolithographic steps several techniques appropriate for a low-cost process have been investigated. The rear emitter can be locally milled off with the same dicing device used for the creation of the holes (Fig. 2). It can also be removed by laser scribing. Within the third method, the unwanted rear emitter is removed after completion of the metallization: in a plasma etching process the two contact grids are used as diffusion barrier during the emitter formation; a method which allows a higher open circuit voltage, thanks to better surface passivation properties.

IV. CELL PROCESSING

Every process starts with the formation of the connecting holes. After wet chemical removal of the saw damage, the wafers (Cz Si, 1 $\Omega$cm, thickness: 330 $\mu$m, cell size: 5 $\times$ 5 cm$^2$) are submitted to an n$^+$-diffusion. Depending on how the definition of the rear side p/n-area is carried out, an SiN layer at the later base region serves as diffusion barrier. POCl$_3$ open tube diffusion as well as phosphorus doping pastes diffused in a conveyor belt infrared furnace were applied. As a result, the whole cell surface including the inner walls of the holes were covered by an n$^+$-doped layer. The definition of the interdigitated p- and n-type regions followed as described above. During the subsequent screen printing metallization, a relatively relaxed alignment in the range of 100 $\mu$m has to be carried out; it can be automatically done applying the latest screen printers. To accomplish the contact formation, the base and emitter grids are cofired in a commercial infrared firing furnace. Cells, which are still shunted by the rear emitter, i.e., the rear emitter has not yet been removed, are now submitted to plasma etch or to laser scribing. As an option, an anti-reflection coating is deposited on the front side. Thus, the whole process includes only two high-temperature steps and no crucial alignment which is often required by, for example, photolithographically defined structures. Reference cells with a standard solar cell design were processed in parallel.

V. RESULTS AND CHARACTERIZATION

An increase in $J_{SC}$ of 15% was measured compared to the reference cell (Table I), which is mainly due to reduced shadowing losses of the grid-free front side. The EWT holes are covering only 0.6% of the total cell area and therefore are a negligible optical loss factor. For better comparison, no ARC was applied.

Furthermore, the beneficial influence of the rear side emitter is very well visible in an light-beam-induced-current (LBIC) scan (Fig. 3). The graph is generated by illuminating the front of an EWT cell with a small laser spot. The LBIC signal depends on the collection probability which is directly connected to the emitter structure of the device.

However, in contrast to the enhancement of the photocurrent, the open circuit voltage $V_{OC}$ and the fill factor (FF) did not improve. $V_{OC}$ decreases by 2–11% and seems to be related to the insufficiently passivated transition region between neighboring n- and p-doping areas at the cell rear. This supposition is suggested by the observed increase of the dark current $I_{D}$ and confirmed by computer simulations. The application of a silicon nitride layer as diffusion barrier minimizes this decrease in $V_{OC}$. In this case, the critical region, where the pn-junction meets the rear cell surface, moves under the passivating SiN-layer during the emitter diffusion. Investigations showed that this passivating effect cannot be

| Table I | RESULTS OF DIFFERENTLY PROCESSED EWT-BACK-CONTACT-CELLS WITHOUT ARC |
|----|------------------|---------|---------|---------|
| FF [%] | J$_{SC}$ [mA/cm$^2$] | $V_{OC}$ [mV] | $\eta$ [%] | $I_{D}$ [A/cm$^2$] |
| Milling of rear emitter | 61.1 | 23.7 | 541 | 7.8 | $6\times10^{-1}$ |
| Plasma etch, self aligned | 63.4 | 24.3 | 551 | 8.5 | $4\times10^{-1}$ |
| SiN defined p-are | 63.6 | 24.7 | 581 | 9.1 | $5\times10^{-1}$ |
| Conventional cell | 75.6 | 21.4 | 592 | 9.6 | $1\times10^{-1}$ |
attained by a post-diffusion SiN coating. Free charges in the SiN, which are saturated during the P-diffusion, would induce an inversion channel [12] and lead to low shunts (<100 Ω cm²).

Even so, the efficiency of one of our best low-cost EWT-cells within this process reached 12.2% with a suboptimal single plasma enhanced chemical vapor deposition (PECVD) ARC. This is the highest efficiency so far reported for low-cost EWT solar cells [12].

Still, the fill factors are far from being satisfying. The significant drop in FF is caused by several effects:

First, a too-low shunt resistance, easy to determine, causes a considerable loss in FF. A current study to localize the mechanism of shunt formation by a method based on the temperature differences caused by leakage currents showed no relation between the shunt and the EWT-design [13].

Second, an enhanced series resistance severely reduces the FF. The low specific conductivity of the commercial metallization paste used for the base contact is one of the major contributors to the total series resistance. The voltage drop in the base fingers was measured to be 5–10 times higher than in the emitter fingers. Additionally, the series resistance is increased due to a higher contact resistance at the base contact and due to the slightly longer path for an electron generated at the front emitter to the current collecting fingers at the cell rear. Recent calculations showed that this part could be reduced by half within an optimized grid design.

Third, the higher dark current caused by the nonoptimal passivation of the pn-transition region at the rear surface leads to a lower FF.

VI. SIMULATIONS

Simulations were done with the semiconductor device simulation program DESSISTM assuming input parameters (emitter profile, contact distance, etc.) as determined by the applied process. The EWT cell was simulated by a two-dimensional (2-D) unit cell.

The higher the surface recombination velocity (SRV) at the transition region between neighboring n- and p-doped regions, the lower the open circuit voltage (Fig. 4) of the simulated cell and the higher the second dark current $I_{02}$ (Fig. 5). Very similar current–voltage ($I-V$) curves are obtained if a conventionally processed cell is successively perforated by small cuts, which was done to test the negative influence of an unpassivated pn-junction at the surface [14]. A comparison between simulated and experimental data for $V_{oc}$ and FF implies that the prediffusion SiN layer reduces the SRV by a factor of 100.

The growing importance of the surface passivation with the increasing length of the border between two neighboring doping regions is shown in Fig. 4. This length is about a factor of 20 longer for interdigitated p- and n-type doping areas of EWT back contact solar cells compared to the pn-junction at the perimeter of an ordinary cell.

The increased $I_{02}$ results in an approximate loss of 5% (absolute) in FF for the SiN-passivated cell rear.
VII. CONCLUSION

The realization of a back contact EWT-cell design within a low-cost process suitable for an industrial production was demonstrated applying different techniques for p/n-area definition and high throughput formation of the interconnecting holes. The best results with an efficiency of 12.2% on Cz Si (cell size: 25 cm²) were obtained using a laser to drill the holes and PECVD SiN as diffusion barrier for the definition of the base contact areas. Photo-current was measured to be distinctly increased by 15% relative, whereas the FF and open circuit voltage are still to be improved. FF and V_{oc} are lowered due to recombination at the transition region between neighboring p- and n-type doping regions. This loss can be minimized by the passivating effect of the SiN layer. The FF is additionally decreased by considerable low shunt and high series resistances. V_{oc} and FF will be increased by a better rear side passivation and a lower series resistance using an optimized base metallization and grid. In contrast to a conventional cell design, the optimization of the front emitter is not limited by requirements of the screen printing solar cell metallization, which enables the usage of a very shallow and lightly doped emitter structure. This will provide a considerable potential for an increase of the cell efficiency. It is expected that the efficiencies of low-cost back contact EWT cells in their presented design will exceed 15% when incorporating these improvements.

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REFERENCES


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