From equation (11.4), with $V_{sp}$ approximately equal to $V_{THN}$, $\beta_n$ should be far larger than $\beta_p$. In a basic inverter, for both NMOS and PMOS, the length of devices is same and $W_n = 400\mu m$, $W_p = 3\mu m$. Assume $K_p n = 3K_p p$, $V_{DD} = 5V$, $V_{THN} = V_{THF} = 0.9V$, $V_{SP} = (20V_{THN} + V_{DD} - V_{THF})/(1+20) \approx 1.05V$

PMOS: $3/2$, NMOS: $400/2$

While doing simulation, need to use the DC sweep to observe the $V_{sp}$.

Problem 11.2

With $W = 10\mu m$ and a load capacitance of $1pF$, $C_{in} = 1pF + 2 \times 10 \times 2 \times 800aF = 1.032pF$, $R n = 12k\Omega \times 2/10 = 2.4k\Omega$, $R p = 7.2k\Omega$. The propagation delay times are $t_{PHL} = 2.4k\Omega \times 1.032pF \approx 2.5ns$, $t_{PLH} = 7.2k\Omega \times 1.032pF \approx 7.43ns$

Vin is $V_{pulse}$, whose parameters are: 0 5 1ns 0 0 10ns 20ns (not unique, you can use whatever proper parameters for the Vin)
Problem 11.3

For minimum size inverter, \( t_{PH} + t_{FLH} = 160k \times C_{ok} = 160k\Omega \times 4.8fF = 768ps \). Using 31 inverters, the oscillation frequency is 
\[ f_{osc} = \frac{1}{31 \times 768ps} \approx 42\text{MHz}. \]

Problem 12.1

Solution: a) Design and hand-cal: The 2-input CMOS AND gate circuit diagram is shown below which consists of two parts NAND and INVERTOR cascaded:

To find \( V_{sp} \), tie input A and B together as \( V_{in} \). From NAND gate part, ignoring the body effect, we have

\[
V_c = V_{in} = V_{sp} = \frac{\sqrt{\beta_n}}{4\beta p} V_{thn} + (V_{dd} - V_{thp}) \\
1 + \frac{\beta_n}{4\beta p}
\]

(12.1a)

\[
V_{out} = V_c = V_{sp} = \frac{\sqrt{\beta_n}}{4\beta p} V_{thn} + (V_{dd} - V_{thp}) \\
1 + \frac{\beta_n}{4\beta p}
\]

(12.1b)

\( V_{thn} = 0.83\text{V} \), \( V_{thp} = 0.91\text{V} \), choosing all the length of CMOS \( L=2u \), all \( W_p=3u \) for p-channel. Let both \( V_{sp} \) expression equals to 1.5 V, \( \Longrightarrow \) \( W_4=W_5=60u \), \( W_6=15u \).
Again, While doing simulation to observe Vsp, let Va=Vb=Vin, and DC sweep Vin.
Problem 12.3

Solution: For N-input NOR gate, we have:

\[ t_{PHL} = NRp(Coup / N + NCoutr + Cload) + 0.35RpCimp(N - 1)^2 \]  \hspace{1cm} (12.3a)

\[ t_{PLH} = (Rn / N)(NCoutr + Coutr / N + Cload) \]  \hspace{1cm} (12.3b)

With minimum size MOSFET, \( Rn=8k\Omega, Rp=24k\Omega, Coutn=Coutr=4.8fF, 
Cimp=7.2fF. \) and 3 input.

a) With Cload=0:

\[ t_{PLH} = 3 \times 24k(4.8f / 3 + 3 \times 4.8f + 0) + 0.35 \times 24k \times 7.2f / (3 - 1)^2 = 1.394ns \]

\[ t_{PHL} = (8k / 3)(3 \times 4.8f + 4.8f / 3 + 0) = 42.67ps \]

b) With Cload=100fF:

\[ t_{PLH} = 3 \times 24k(4.8f / 3 + 3 \times 4.8f + 100) + 0.35 \times 24k \times 7.2f / (3 - 1)^2 = 8.594ns \]

\[ t_{PHL} = (8k / 3)(3 \times 4.8f + 4.8f / 3 + 100) = 309ps \]

It can be seen that for 3-input NOR gate, the \( t_{PLH} > t_{PHL} \), while for 3-input NAND gate, the \( t_{PLH} < t_{PHL} \), also that the maximum delay time of NOR is bigger than the maximum delay time of NAND. Plus we already know that NAND gate has better \( Vsp \) and better noise margins. That is why in CMOS digital design, the NAND gate is used most often.
From the above Figure, $t_{PLH}=5\text{ns}$. Zoom this result (see below), $t_{PHL}=160\text{ps}$